AN2581
Application note

STM32F10xxx TIM application examples

Introduction

This application note is intended to provide practical application examples of the STM32F10xxx TIMx peripheral use.

This document, its associated firmware, and other such application notes are written to accompany the STM32F10xxx firmware library. These are available for download from the STMicroelectronics website: *www.st.com*.

Contents

1 STM32F10xxx TIMx output compare mode

1.1 Overview

This section provides a description of how to configure the TIM peripheral in output compare mode to generate four different signals with four different frequencies.

1.2 Firmware description

The provided firmware includes the TIMx driver that supports all TIMx functionalities through a set of functions. An example of use for most of these functions is provided.

The TIMxCLK frequency is set to 36 MHz, the prescaler is set to 0x2 and used in the output compare toggle mode.

TIM2 counter clock = TIMxCLK / (Prescaler +1) = 12 MHz

The TIM2_CCR1 register value is equal to 0x8000:

CC1 update rate = TIM2 counter clock / CCR1_Val = 366.2 Hz,

so TIM2_CH1 generates a periodic signal with a frequency equal to 183.1 Hz.

The TIM2_CCR2 register is equal to 0x4000:

CC2 update rate = TIM2 counter clock / CCR2_Val = 732.4 Hz

so TIM2_CH2 generates a periodic signal with a frequency equal to 366.3 Hz.

The TIM2_CCR3 register is equal to 0x2000:

CC3 update rate = TIM2 counter clock / CCR3_Val = 1464.8 Hz

so the TIM2_CH3 generates a periodic signal with a frequency equal to 732.4 Hz.

The TIM2_CCR4 register is equal to 0x1000:

CC4 update rate = TIM2 counter clock / CCR4_Val = 2929.6 Hz

so the TIM2_CH4 generates a periodic signal with a frequency equal to 1464.8 Hz.

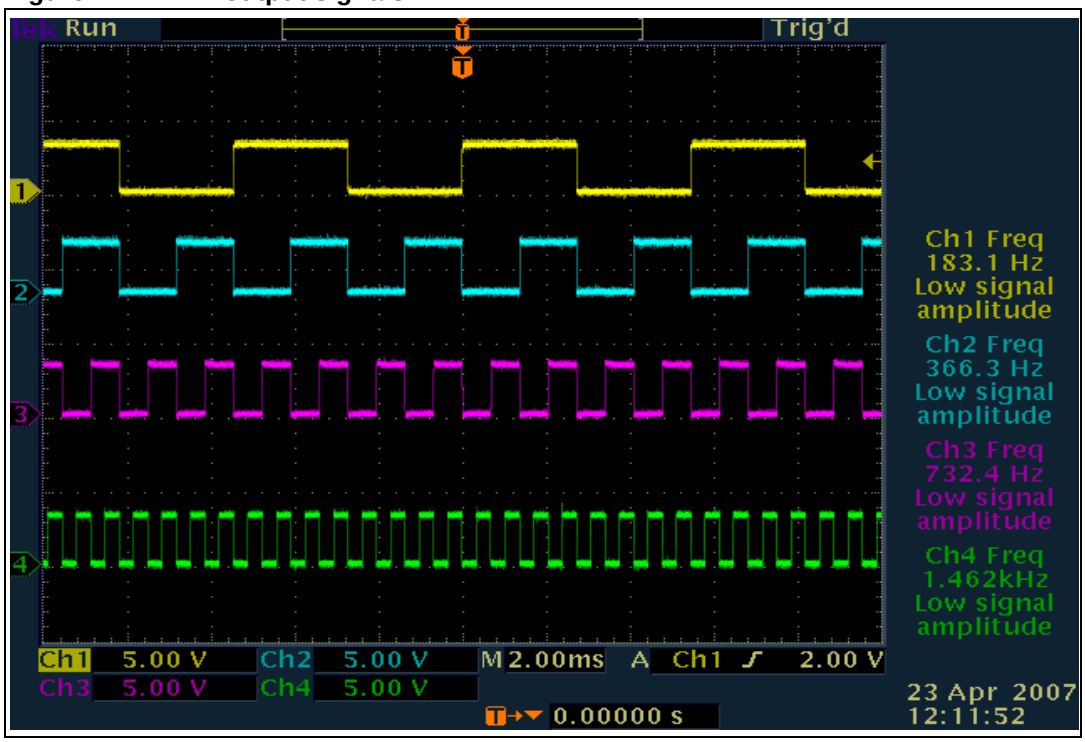
This firmware is provided as *TIM example 1* in the STM32F10xxx firmware library, available from the STMicroelectronics microcontrollers website.

1.3 TIMx output signal behavior

To display the four signals (see *Figure 1*), connect an oscilloscope to the following pins:

- PA0 (TIM2_CH1)
- PA1 (TIM2_CH2)
- PA2 (TIM2_CH3)
- PA3 (TIM2_CH4)

Figure 1. TIM2 output signals



2 Delay generation in TIMx output compare active mode

2.1 Overview

This section provides a description of how to configure the TIM peripheral to generate four different signals with four different delays.

2.2 Firmware description

The provided firmware includes the TIMx driver that supports all TIMx functionalities through a set of functions. An example of use for most of these functions is provided.

The TIMxCLK frequency is set to 36 MHz, the prescaler is set to 35999 and used in the output compare active mode.

TIM2 counter clock = TIMxCLK / (Prescaler +1) = 1 kHz

The TIM2_CCR1 register value is equal to 1000:

TIM2_CH1 delay = CCR1_Val/TIM2 counter clock = 1000 ms

so the TIM2_CH1 generates a signal with a delay equal to 1000 ms.

The TIM2_CCR2 register value is equal to 500:

TIM2_CH2 delay = CCR2_Val/TIM2 counter clock = 500 ms

so the TIM2_CH2 generates a signal with a delay equal to 500 ms.

The TIM2_CCR3 register value is equal to 250:

TIM2_CH3 delay = CCR3_Val/TIM2 counter clock = 250 ms

so the TIM2_CH3 generates a signal with a delay equal to 250 ms.

The TIM2_CCR4 register value is equal to 125:

TIM2_CH4 delay = CCR4_Val/TIM2 counter clock = 125 ms

so the TIM2_CH4 generates a signal with a delay equal to 125 ms.

The delay corresponds to the time difference between the rising edge of the PC6 signal and the rising edge of the TIM2_CHx signal.

This firmware is provided as *TIM example 2* in the STM32F10xxx firmware library, available from the STMicroelectronics microcontrollers website.

2.3 TIMx output signal behavior

To display the four different signals (see *Figure 2*), connect an oscilloscope to:

- PC6
- PA0 (TIM2_CH1)
- PA1 (TIM2_CH2)
- PA2 (TIM2_CH3)
- PA3 (TIM2_CH4)

Figure 2. TIM2 output signals

3 STM32F10xxx TIMx output compare inactive mode

3.1 Overview

This section provides a description of how to configure the TIM peripheral in the output compare inactive mode with the corresponding Interrupt requests for each channel.

3.2 Firmware description

The provided firmware includes the TIMx driver that supports all TIMx functionalities through a set of functions. An example of use for most of these functions is provided.

The TIMxCLK frequency is set to 36 MHz, the prescaler is set to 35999 and used in output compare inactive mode.

TIM2 counter clock = TIMxCLK / (Prescaler +1) = 1 kHz

The TIM2_CCR1 register value is equal to 1000:

TIM2_CC1 delay = CCR1_Val/TIM2 counter clock = 1000 ms

so PC6 is reset after a delay equal to 1000 ms.

The TIM2_CCR2 register value is equal to 500:

TIM2_CC2 delay = CCR2_Val/TIM2 counter clock = 500 ms

so PC7 is reset after a delay equal to 500 ms.

The TIM2_CCR3 register value is equal to 250:

TIM2_CC3 delay = CCR3_Val/TIM2 counter clock = 250 ms

so PC8 is reset after a delay equal to 250 ms.

The TIM2_CCR4 register value is equal to 125:

TIM2_CC4 delay = CCR4_Val/TIM2 counter clock = 125 ms

so PC9 is reset after a delay equal to 125 ms.

While the counter is lower than the Output compare register values that determine the output delay, the PC6, PC7, PC8 and PC9 pins are driven High.

When the counter value reaches the Output compare register values, the Output Compare interrupts are generated and, in the handler routine, these pins are driven Low.

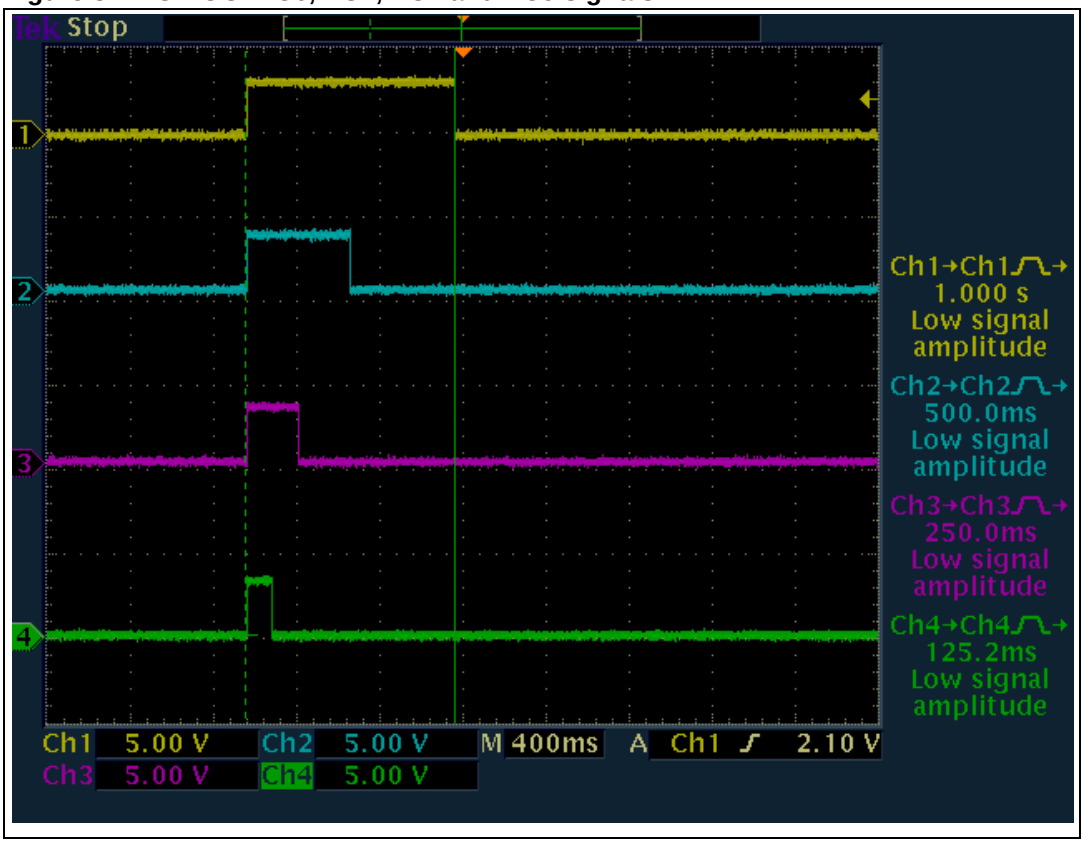
This firmware is provided as *TIM example 3* in the STM32F10xxx firmware library, available from the STMicroelectronics microcontrollers website.

3.3 TIMx output signal behavior

To display the different signals (see *Figure 3*), connect an oscilloscope to:

- PC6 (CH1)
- PC7 (CH2)
- PC8 (CH3)
- PC9 (CH4)

Figure 3. GPIOC: PC6, PC7, PC7 and PC9 signals



4 STM32F10xxx TIMx pulse width modulation mode

4.1 Overview

This section provides a description of how to configure the TIM peripheral in PWM (pulse width modulation) mode.

4.2 Firmware description

The provided firmware includes the TIMx driver that supports all TIMx functionalities through a set of functions. An example of use for most of these functions is provided.

The TIMxCLK frequency is set to 36 MHz, the prescaler is 0 so the TIM3 counter clock frequency is 36 MHz. TIM3 is running at 36 kHz:

TIM3 frequency = TIM3 counter clock/(TIM3_ARR + 1)

The TIM3_CCR1 register value is equal to 0x1F4, so TIM3_CH1 generates a PWM signal with a frequency equal to 36 kHz and a duty cycle equal to 50%:

TIM3_CH1 duty cycle = TIM3_CCR1/ (TIM3_ARR + 1) × 100 = 50%

The TIM3_CCR2 register value is equal to 0x177, so the TIM3_CH2 generates a PWM signal with a frequency equal to 36 kHz and a duty cycle equal to 37.5%:

TIM3_CH2 duty cycle = TIM3_CCR2/ (TIM3_ARR + 1) × 100 = 37.5%

The TIM3_CCR3 register value is equal to 0xFA, so the TIM3_CH3 generates a PWM signal with a frequency equal to 36 kHz and a duty cycle equal to 25%:

TIM3_CH3 duty cycle = TIM3_CCR3/ (TIM3_ARR + 1) × 100 = 25%

The TIM3_CCR4 register value is equal to 0x7D, so the TIM3_CH4 generates a PWM signal with a frequency equal to 36 kHz and a duty cycle equal to 12.5%:

TIM3_CH4 duty cycle = TIM3_CCR4/ (TIM3_ARR + 1) × 100 = 12.5%

The PWM waveform can be displayed using an oscilloscope.

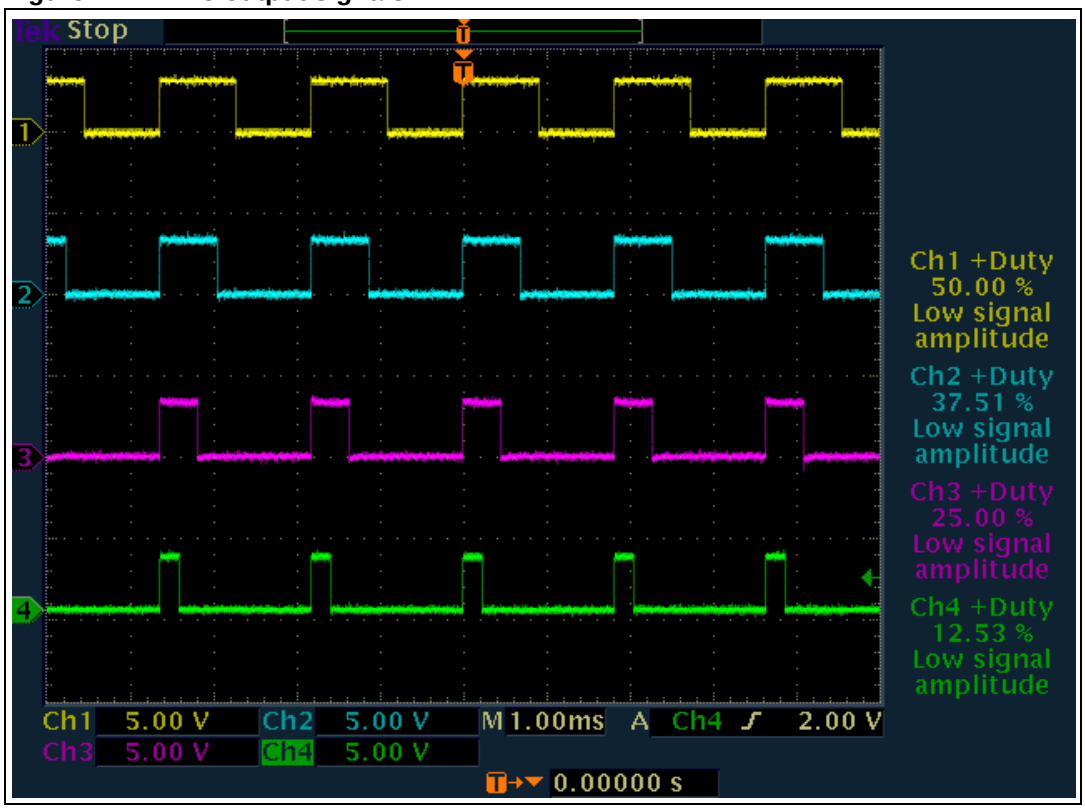
This firmware is provided as *TIM example 4* in the STM32F10xxx firmware library, available from the STMicroelectronics microcontrollers website.

4.3 TIMx output signal behavior

To display the four different signals (see *Figure 4*), connect an oscilloscope to:

- PA6: (TIM3_CH1)
- PA7: (TIM3_CH2)
- PB0: (TIM3_CH3)
- PB1: (TIM3_CH4)

Figure 4. TIM3 output signals



5 TIMx output compare timing mode: time-base generation

5.1 Overview

This section provides a description of how to configure the TIM peripheral in output compare timing mode with the corresponding interrupt requests for each channel in order to generate four different time bases.

5.2 Firmware description

The provided firmware includes the TIMx driver that supports all TIMx functionalities through a set of functions. An example of use for most of these functions is provided.

The TIMxCLK frequency is set to 36 MHz, the prescaler is 0x4 so the TIM2 counter clock frequency is 7.2 MHz.

The TIM2_CCR1 register value is equal to 0xC000

CC1 update rate = TIM2 counter clock / CCR1_Val = 146.48 Hz,

so TIM2_CH1 generates an interrupt every 6.8 ms

The TIM2_CCR2 register is equal to 0x8000,

CC2 update rate = TIM2 counter clock / CCR2_Val = 219.7 Hz,

so TIM2_CH2 generates an interrupt every 4.55 ms

The TIM2_CCR3 register is equal to 0x4000,

CC3 update rate = TIM2 counter clock / CCR3_Val = 439.4Hz,

so TIM2_CH3 generates an interrupt every 2.27 ms

The TIM2_CCR4 register is equal to 0x2000,

CC4 update rate = TIM2 counter clock / CCR4_Val = 878.9 Hz,

so TIM2_CH4 generates an interrupt every 1.13 ms.

When the counter value reaches the Output compare register values, the Output Compare interrupts are generated and, in the handler routine, 4 pins (PC6, PC7, PC8 and PC9) are toggled at the following frequencies:

- PC6: 73.24 Hz (CC1)
- PC7: 109.8 Hz (CC2)
- PC8: 219.7 Hz (CC3)
- PC9: 439.4 Hz (CC4)

This firmware is provided as *TIM example 5* in the STM32F10xxx firmware library, available from the STMicroelectronics microcontrollers website.

5.3 TIMx output signal behavior

Connect an oscilloscope to PC6, PC7, PC8 and PC9 to display the different time-base signals as shown in *Figure 5*.

Figure 5. GPIOD signals: PC6, PC7, PC8 and PC9

6 STM32F10xxx TIMx PWM input mode

6.1 Overview

This section provides a description of how to use the TIM peripheral to measure the frequency and duty cycle of an external signal.

6.2 Firmware description

The provided firmware includes the TIMx driver that supports all TIMx functionalities through a set of functions. An example of use for most of these functions is provided.

The TIMxCLK frequency is set to 72 MHz, the prescaler is 0x0 so the TIM2 counter clock frequency is 72 MHz. So the minimum frequency value to measure is 1100 Hz.

TIM2 is configured in PWM input mode: the external signal is connected to TIM2_CH2 (PA1) used as the input pin. To measure the frequency and duty cycle, the TIM2 CC2 interrupt request is used, so in the TIM2_IRQ handler routine, the frequency and duty cycle of the external signal are computed.

The "Frequency" variable contains the external signal frequency:

Frequency = TIM2 counter clock / TIM2_CCR2 in Hz,

The "Duty_Cycle" variable contains the external signal duty cycle:

Duty_Cycle = (TIM2_CCR1*100)/(TIM2_CCR2) in %.

This firmware is provided as *TIM example 6* in the STM32F10xxx firmware library, available from the STMicroelectronics microcontrollers website.

7 Generating an OPM waveform after an edge on TIMx TIx input

7.1 Overview

This section provides a description of how to use the TIM peripheral to generate an OPM (one pulse mode) waveform after the rising edge of an external signal is received on the timer input pin (TI).

7.2 Firmware description

The provided firmware includes the TIMx driver that supports all TIMx functionalities through a set of functions. An example of use for most of these functions is provided.

The TIMxCLK frequency is set to 72 MHz, the prescaler is 0x1 so the TIM2 counter clock frequency is 36 MHz.

The autoreload value is 0xFFFF (TIM2_ARR), so the maximum frequency value to trigger the TIM2 input is 500 Hz.

TIM2 is configured as follows: the one pulse mode is used, the external signal is connected to the TIM2_CH2 pin (PA1), the rising edge is used as the active edge, the one-pulse signal is output on TIM2_CH1 (PA0).

TIM_Pulse defines the delay value that is fixed to 455.08 µs:

delay = CCR1/TIM2 counter clock = 455.08 µs

(TIM_Period - TIM_Pulse) defines the one-pulse value, the pulse value is fixed to 1.365 ms:

One-pulse value = (TIM_Period - TIM_Pulse)/TIM2 counter clock = 1.365 ms

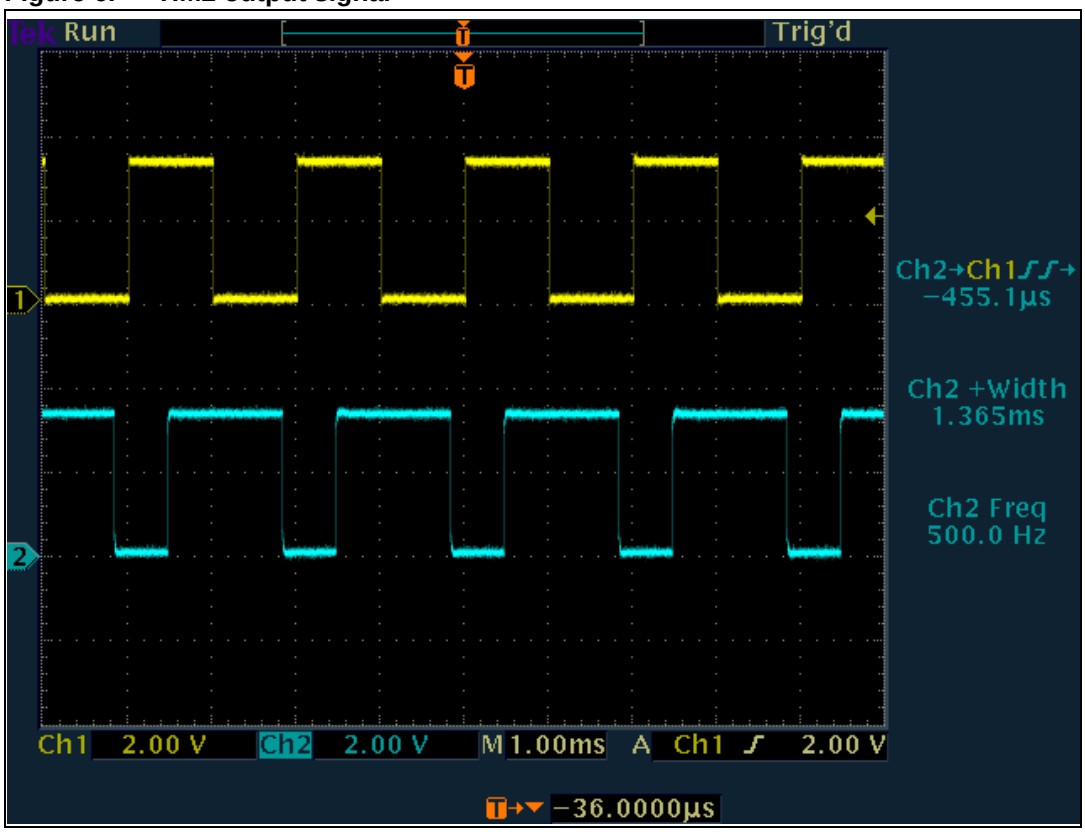
This firmware is provided as *TIM example 7* in the STM32F10xxx firmware library, available from the STMicroelectronics microcontrollers website.

7.3 TIMx output signal behavior

Connect the external signal to measure to the TIM2 CH2 pin (PA1). Connect the TIM2_CH1 (PA0) pin to an oscilloscope to show the waveform.

In *Figure 6*, the Ch1 presents the input signal triggering TIM2 and Ch2 is connected to TIM2_CH2 and presents the TIM2 one-pulse signal.

Figure 6. TIM2 output signal



8 Synchronizing TIMx peripherals in parallel mode

8.1 Overview

This section provides a description of how to synchronize TIMx peripherals in parallel mode.

8.2 Firmware description

The provided firmware includes the TIMx driver that supports all TIMx functionalities through a set of functions. An example of use for most of these functions is provided.

Timer synchronization in parallel mode:

1. TIM2 is configured as the master timer:
   - PWM mode is used
   - The TIM2 update event is used as the trigger output
2. TIM3 and TIM4 are slaves for TIM2
   - PWM mode is used
   - ITR1 (TIM2) is used as the input trigger for both slaves
   - Gated mode is used, so starts and stops of slave counters are controlled by the master trigger output signal (update event)

The master timer, TIM2, is running at 281.250 kHz and the duty cycle is equal to 25%.

The TIM3 is running at:

(TIM2 frequency) / (TIM3 Period + 1) = 28.1250 kHz

and its duty cycle is equal to:

TIM3_CCR1/(TIM3_ARR + 1) = 30%

The TIM4 is running at:

at (TIM2 frequency) / (TIM4 Period + 1) = 56.250 kHz

and its duty cycle is equal to:

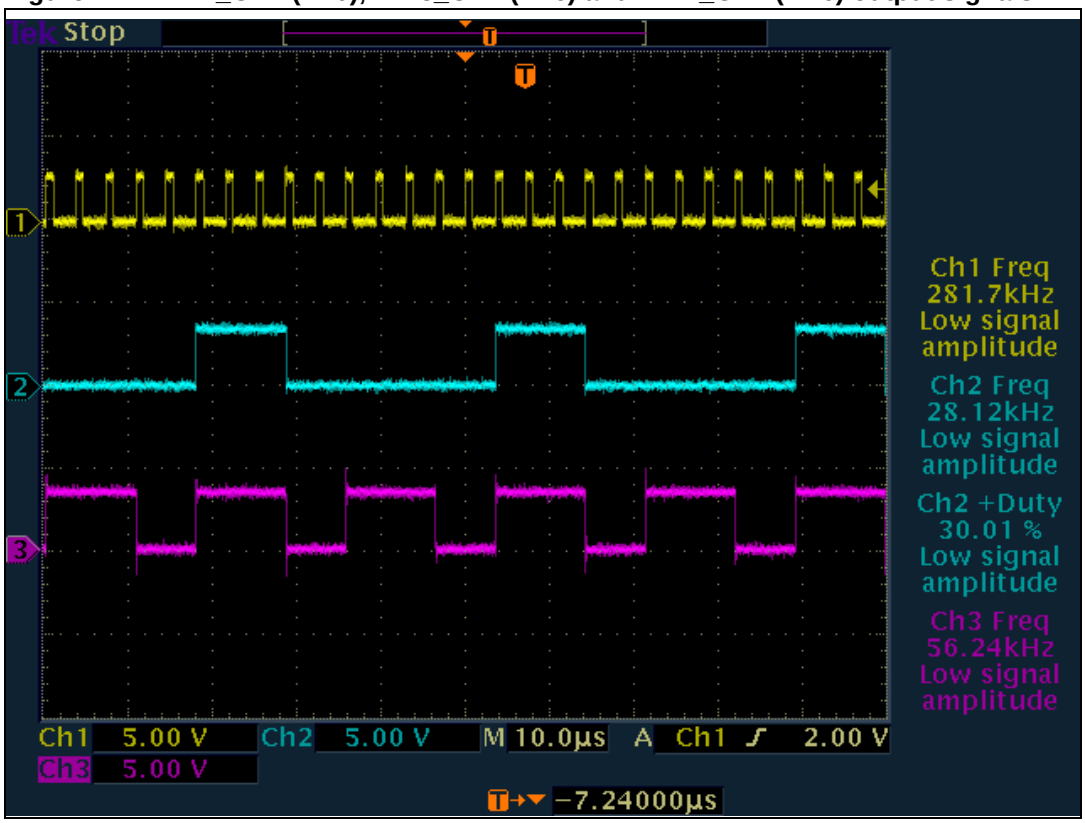
TIM4_CCR1/(TIM4_ARR + 1) = 60%

This firmware is provided as *TIM example 8* in the STM32F10xxx firmware library, available from the STMicroelectronics microcontrollers website.

8.3 TIMx output signal behavior

Connect the TIM2_CH1 (PA0), TIM3_CH1 (PA6) and TIM4_CH1 (PB6) pins to an oscilloscope to display the waveforms (see *Figure 7*).

Figure 7. TIM2_CH1 (PA0), TIM3_CH1 (PA6) and TIM4_CH1 (PB6) output signals



9 Synchronizing TIMx peripherals in cascade mode

9.1 Overview

This section provides a description of how to synchronize TIM peripherals in cascade mode.

9.2 Firmware description

The provided firmware includes the TIMx driver that supports all TIMx functionalities through a set of functions. An example of use for most of these functions is provided.

Timer synchronization in cascade mode:

1. TIM2 is configured as the master timer:
   - PWM mode is used
   - the TIM2 update event is used as the trigger output
2. TIM3 is a slave for TIM2 and the master for TIM4:
   - PWM mode is used
   - ITR1 (TIM2) is used as the input trigger
   - Gated mode is used, so starts and stops of the slave counter are controlled by the master trigger output signal (TIM2 update event)
   - The TIM3 update event is used as the trigger output.
3. TIM4 is a slave for TIM3:
   - PWM mode is used
   - ITR2 (TIM3) is used as the input trigger
   - Gated mode is used, so starts and stops of the slave counter are controlled by the master trigger output signal (TIM3 update event)

The TIMxCLK is fixed to 72 MHz, the TIM2 counter clock frequency is 72 MHz.

The master timer, TIM2, is running at the TIM2 frequency:

TIM2 frequency = (TIM2 counter clock)/ (TIM2 Period + 1) = 281.250 kHz and

duty cycle = TIM2_CCR1/(TIM2_ARR + 1) = 25%.

The TIM3 is running at:

(TIM2 frequency)/ (TIM3 Period + 1) = 70.312 kHz and

duty cycle = TIM3_CCR1/(TIM3_ARR + 1) = 25%

The TIM4 is running at:

(TIM3 frequency)/ (TIM4 Period + 1) = 17.578 Hz and

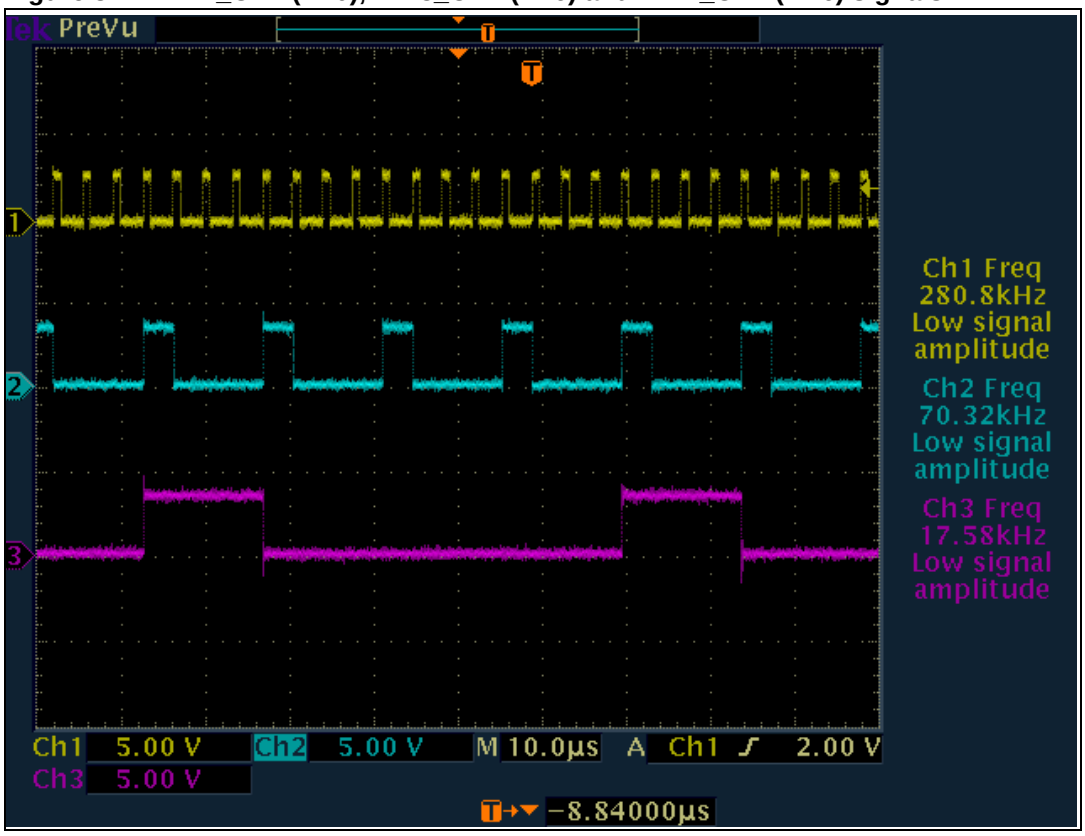
duty cycle = TIM4_CCR1/(TIM4_ARR + 1) = 25%

This firmware is provided as *TIM example 9* in the STM32F10xxx firmware library, available from the STMicroelectronics microcontrollers website.

9.3 TIMx output signal behavior

Connect the TIM2_CH1 (PA0), TIM3_CH1 (PA6) and TIM4_CH1 (PB6) pins to an oscilloscope to display the waveforms (see *Figure 8*).

Figure 8. TIM2_CH1 (PA0), TIM3_CH1 (PA6) and TIM4_CH1 (PB6) signals



10 Synchronizing several timers TIMx to an external trigger

10.1 Overview

This section provides a description of how to synchronize TIMx peripherals in cascade mode to an external trigger.

10.2 Firmware description

The provided firmware includes the TIMx driver that supports all TIMx functionalities through a set of functions. An example of use for most of these functions is provided.

Timer synchronization in cascade mode with an external trigger:

1. TIM2 is configured as the master timer:
   - Toggle mode is used
   - the TIM2 enable event is used as the trigger output
2. TIM2 is configured as a slave timer for an external trigger connected to the TIM2 TI2 pin (TIM2_CH2 configured as an input pin):
   - TIM2 TI2FP2 is used as the trigger input
   - rising edge is used to enable and stop TIM2: gated mode
3. TIM3 is a slave for TIM2 and the master for TIM4,
   - Toggle mode is used
   - ITR1 (TIM2) is used as the input trigger
   - Gated mode is used, so starts and stops of the slave counter are controlled by the master trigger output signal (TIM2 enable event)
   - the TIM3 enable event is used as the trigger output
4. TIM4 is a slave for TIM3
   - Toggle mode is used
   - ITR2 (TIM3) is used as the input trigger
   - Gated mode is used, so starts and stops of the slave counter are controlled by the master trigger output signal (TIM3 enable event)

TIMxCLK is fixed to 72 MHZ, the prescaler is equal to 0x2 so the TIMx clock counter frequency is 24 MHz.

The three timers are running at:

TIMx frequency = TIMx clock counter/ 2 × (TIMx_Period + 1) = 162.1 kHz

The starts and stops of the TIM2 counter are controlled by the external trigger. TIM3 starts and stops are controlled by TIM2, and TIM4 starts and stops are controlled by TIM3.

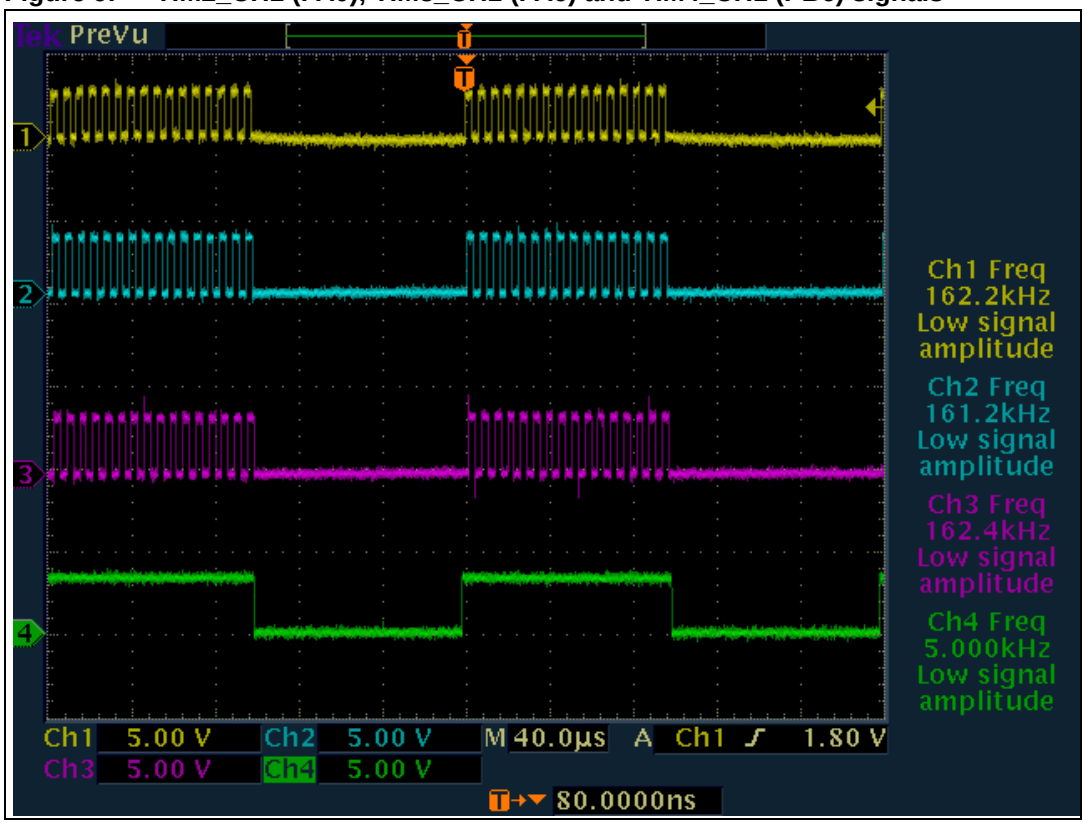
This firmware is provided as *TIM example 10* in the STM32F10xxx firmware library, available from the STMicroelectronics microcontrollers website.

10.3 TIMx output signal behavior

Connect an external trigger with a frequency lower than or equal to 40 kHz, to the TIM2_CH2 pin. In this example the frequency is equal to 5 kHz.

Connect the TIM2_CH1 (PA0), TIM3_CH1 (PA6) and TIM4_CH1 (PB6) pins to an oscilloscope to display the waveforms (see *Figure 9*).

Figure 9. TIM2_CH1 (PA0), TIM3_CH1 (PA6) and TIM4_CH1 (PB6) signals



11 Revision history

Table 1. Document revision history

Date	Revision	Changes
26-Jun-2007	1	Initial release.

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