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Spice Model for TMOS Power MOSFETs

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INTRODUCTION

The "Microcomputer Boom" allows designers to run performance programs with rather low investments in personal computers such as IBM PC, PS, Macintosh and other stations with graphic terminals. SPICE was one of the simulation programs which was formerly available only on main computers but now can be used on personal computers.

In power electronics, being able to simulate the power dissipation is key for a designer. Up to now, very few solutions by simulations have been possible, primarily because both component and programming experience was required. A university in Toulouse, France (LAAS-CNRS) and a component manufacturer (Motorola) put their efforts together to build a power MOSFET (TMOS) library to solve this problem. A library has been conceived that is as universal as possible and can be implemented in different programs.

What is SPICE?

SPICE is a general purpose circuit simulation program for non-linear DC, non-linear transient and linear AC analyses resolving nodes matrix. Circuits may contain resistors, capacitors, inductors, mutual inductors, independent voltage and current sources, four types of semiconductor devices: diodes, BJTs, JFETs and MOSFETs. This program was first developed by the Department of Electrical Engineering and Computer Sciences of Berkley, University California. The use of a very basic language already made it user friendly, but the availability of additional programs around SPICE for schematic capture or post-processing now simplifies the designer's work and gives him, for example, the familiar oscilloscope and drawing board similar to the ones he is accustomed to using in his lab. Since the SPICE source program is now available on the market, software companies have developed new versions with their own models. It could take too long to quote all them, but some like SPICE2G6, P-SPICE, H-SPICE, etc. are already well known.

TMOS is a trademark of Motorola Inc.
H-SPICE is a trademark of META Software
P-SPICE is a trademark of Microsim Corp.
Microsoft is a registered trademark of Microsoft Corp.

What can SPICE and the TMOS Library do for you in Power Applications?

It saves time and produces accurate circuit simulations. For example, on short notice, you're asked to determine the performance of a schematic (Figure 1) with different voltage, current and timing conditions. Like most engineers, you are very busy and dislike doing such testing in a hurry, because, by experience, you know it's not possible to set up and take thorough measurements required in the timeframe.

What can you do?

— tell your superior that it's not possible to get a thorough evaluation in the timeframe allowed,
— tell him he has to change your priorities because you are already overloaded,

OR

use SPICE and the TMOS Library and in half an hour the job is done. The following morning, you have the oscillograms similar to the one shown in Figure 19. Now selections can be made from a limited number of voltage, current and timing conditions for bench testing.

Because of their wide diffusion, simulation programs have become very popular and most of the students coming from electronic universities and engineering schools

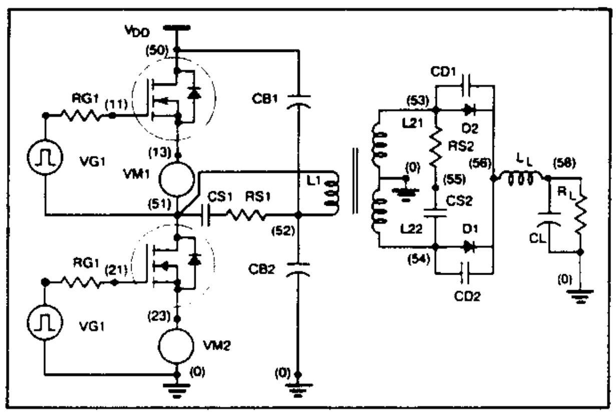

Figure 1. Typical Application for SPICE Using Power Elements

This application note is intended for those familiar with simulation programs such as SPICE, SPICE2G6, P-SPICE, H-SPICE or similar simulation programs. The information in this note has been carefully checked and believed to be accurate, however, no responsibility is assumed for inaccuracies.

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are familiar with them. Simulation programs like SPICE allow them to verify the functionalty of their circuit before going to the bench. Time saving is one advantage. Another is to mimimize the hazards of bench failure. SPICE simulations do not go up in smoke or explode if a mistake or miscalculation is made, whereas mistakes during bench testing can result in smoke or explosions with power products.

Most students today are oriented toward small signal, digital or analog designs, therefore they are not accustomed to dealing with high currents and high voltages. A tool like SPICE can make power electronics more friendly to them. It is especially true when a circuit designer for logic has to check the interaction of his circuit with the power switches to be driven. For instance, it is known that signal perturbations caused by the Miller capacitance of power MOSFETs can make logic circuits driving power MOSFETs malfunction. Being able to simulate such phenomena prior to bench testing reduces the design cycle time and results in more reliable systems.

The major drawback of SPICE for power electronic engineers is that it is dedicated to small signal analysis. In any of the SPICE versions, there is no simple model for a power transistor, whether it is bipolar transistor or a power MOSFET. Some software firms provide some data, but you have to purchase the program where the new model has been compiled. A few firms provide the option of writing the model yourself in Fortran or C language.

Because our goal was to have the model work on any SPICE version (compatible with SPICE2G6), the only way to achieve it was to use the existing components available on all versions and build a subcircuit library which could be called from the main circuit program.

What was the goal of this study and its limits?

The study made with LAAS/CNRS lab in Toulouse consists of modeling around twenty power MOSFETs.

The study proposed was to be pragmatic, that is to say a step by step approach. Our primary goal was to have a model fully working at 25°C under static and dynamic conditions. The twenty transistors studied, two of which were P-channel devices have been tested in inductive and resistive switching tests as well as DC analysis. Parameter extraction has been performed with one or two products of each type which can be assumed to be typical of today's line. Data sheets are not as accurate as measurements and are just used for verification.

The thermal aspects will be taken into account in a future study. This will require some new techniques because SPICE only allows the whole circuit temperature study and does not take into account the temperature rise of the power product alone. Parameters like thermal resistances and thermal capacitances will have to be introduced in another manner or will have to be added in the models. This will require a whole revision of the source program to take into account these aspects and work at the equation level.

This document contains:

I. A User Manual

For those who want to get started first and are not concerned about the device physics. It explains how to use the content of the floppy disk.

II. The Physics of the Power MOSFET

A description of the physical model and the simplifications performed.

III. Implementation of the Model for SPICE Program

Taking into account differences between low and high voltage TMOS power MOSFETs.

IV. The Parameters Extraction Method

An overview on how the parameters have been extracted and how the user could extract them.

V. The Results

A comparison between simulation and measurement is given for some test configurations and applications.

TABLE OF CONTENTS

I. USER MANUAL

This chapter contains material for people who are already accustomed to SPICE programming and would like to know the contents of the floppy disk and how to use it.

For use with this Application Note, floppy disks are available that are format compatible with IBM PC or Macintosh micro computers. Simply indicate which disk you need by completing the attached card and returning it to Motorola.

Order DK103/D for the 5¼" disk for 360Kb IBM PC compatible*
Order DK202/D for the 3½" disk for 800Kb Macintosh (double side)*
Order DK301/D for the 3½" disk for 720Kb IBM PC compatible (double side)*

All of this material has been developed with PSPICE of MicroSim Corp., but since all the data contained in this disk are ASCII files, they can be read by any word processor and modified for the context of the user. As you'll notice, the **.PROBE** command helps us to see the displays on the screen. If you do not have this feature, you can use **.PRINT** or **.PLOT** for other output formats.

The floppy disk contains different files. The first three are are dedicated to the Motorola power MOSFET library itself. They can be used directly with any SPICE2G6 compatible version without any change. The other programs may require some changes if you do not use PSPICE. But in any case, you can list them with any editor program and change the syntax to have it compatible with your own SPICE version: you may have to replace **.PROBE** by **.PLOT** and maybe the syntax of some calls (e.g. **I(X1.RS)**).

A. The TMOS library

1. What Is On the Disk

TMOS.LIB

This file is the most useful one, using a model with switched capacitors and requiring no initialization (Figure 2). Starting with this disk is advised, even though it might be a little slow. The schematic for the P-channel model is given in the Appendix.

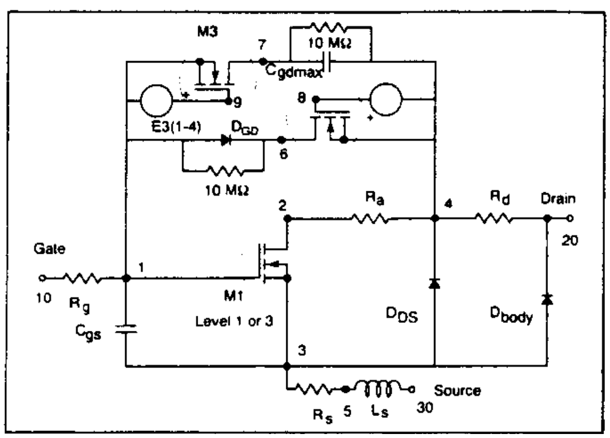

Figure 2. Block Diagram of the N-Channel TMOS Model Used in TMOS.LIB

TMOSINIT.LIB

This is, from the static point of view, exactly the same as the previous file, but is much faster since it does not use the capacitor switches (Figure 3). The drawback is that it requires an initialization step for the node (6) between $C_{GD}max$ and D_{GD} (only for the transient analysis).

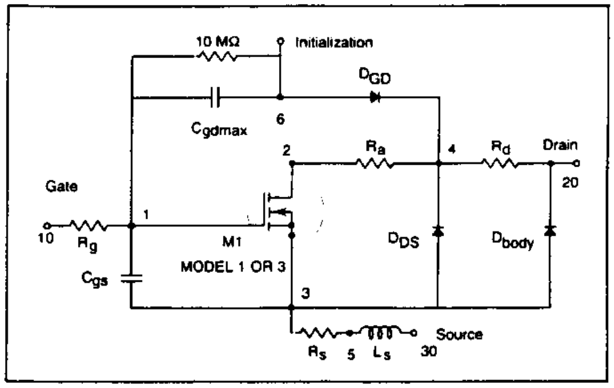

Figure 3. Block Diagram of the N-Channel TMOS Model Used in TMOSINIT.LIB

The voltage of this node depends on the V_{DS} and V_{GS} voltages at the start of the simulation. Therefore a utility file called **INIT.CIR** is provided with this TMOSINIT library.

INIT.CIR

This SPICE compatible file helps you to compute the initial condition V(8) to set on node 6 for the given starting V_{DS} (Figure 4).

```
Program for initialization values of MTP3055E
*this program can be used to determine initialization
value to be put on node (6) when using TMOSINIT
library with the two capacitances in series

*please enter the part number you want to work with.
and adjust the max voltage desired
*****************************************************
X1 2 0 0 8 MTP3055E
VDS 2 0 PULSE(0 50 0U 500N 20N 0.5U 1U)
*****************************************************
.LIB TMOSINIT.LIB
.TRAN 10N 500N 0N
.PRINT TRAN V(2) V(8)
.PROBE V(2) V(8)
.END
```

Figure 4. Description of the Initialization Routine Called INIT.CIR to be Used With TMOSINIT.LIB

2. How to Call a Device In the Library

a. For the **TMOS.LIB** library you'll need to write in your source program:

.LIB TMOS.LIB *to call the library with switched capacities*

*These disks are formatted and require the software Microsoft Word version 3.02 or newer

X1 MTP25N06 2 1 3 *to call the product to be used*

```
!              ! ! !
!              ! Source
!              !Gate
!              Drain
Device Part Number available in the library
```

b. If you use **TMOSINIT.LIB** you'll need:

.LIB TMOSINIT.LIB *to call the faster but more complex library*

X1 MTP25N06 2 1 3 8 *to call the product to be used*

```
!              ! ! ! !
!              ! ! ! Initialization pin (node 6 between
                     CGDMAX and DGD)
!              ! ! Source
!              ! Gate
!              Drain
!Device Part Number available in the library
```

.IC V(8)=2.5 *The voltage value of the extrinsic node 8 will be given by the* ***INIT.CIR*** *program according to the V_{DS} voltage at the initialization phase. If you do not enter the proper value, it may give you incorrect switching times.*

3. Additional Information on the Library

Both **TMOS.LIB** and **TMOSINIT.LIB** have been created so you do not need to modify them. They work for both DC and transient analysis. The latter one needs to be initialized.

One of your concerns at this point of the reading, may be to know what is given: either the typical values or the maximum ratings. Typical values of today's products measured at 25°C are given.

The library has been done from the measurements on one or two products of every part number, and they can be considered typical of the product line. These have been checked and are within the data sheet limits. The simulation is accurate in the range of 80 to 90%.

The comparison with the data sheet curves can be done too, but with some care. The user may not have the updated document and the products may have been improved, therefore some differences may be found between the SPICE simulation and the data sheet curves.

In the chapter called Parameters Extraction Method (Section IV), we will see how the library was built and also, how to modify it if the user wants the simulation with min/max parameter values rather than the typical ones.

B. Validation Programs or Testbox

This file contains some tools to evaluate the library. You are welcome to use them and modify them to your own needs. They are component manufacturer oriented, which means they tend more to simulate the data sheet curves rather than the application, but you'll find some typical applications circuits also. Please refer to the Appendix for the description of the schematic of the following files.

1. **ONCHARAC.CIR**

One of the first curves you find in the data sheets is On-Region characteristics. It gives the drain current (I_D) versus the drain-source voltage (V_{DS}) for different gate-source voltages (V_{GS}). Only a DC analysis is required for such a test and it requires a very small amount of program lines. (see Appendix). For other devices, you just need to change the device part number using the Find/Replace option of your editing program.

For example:
Find: MTP25N06
Replace by: MTP3055E REPLACE ALL

2. **ID-VGS.CIR**

It gives you the transfer characteristic curve: drain current (I_D) versus gate-source voltage (V_{GS}) for a given drain-source voltage (V_{DS} generally equal to 10 volts). This is one more DC test.

3. **RDSON.CIR**

It gives the ON state resistance for different drain current values. The ratio V_D/I_D must be put on the y-axis to get the data sheet curve.

4. **CAPACITY.CIR**

This is the first program out of several using the transient analysis option of SPICE to check the dynamic response of the TMOS model. **CAPACITY.CIR** gives you the capacitance variation curve of the power MOSFET. This curve is difficult to measure and requires a rather sophisticated bench setup (like BOONTON or HP). Therefore you'll have to rely on the data sheet curves.

The principle of this test in SPICE is based on the capacitor equation:

$$i(t) = C(t)\frac{dv}{dt}$$

If a voltage increase, with a constant dv/dt is applied on a linear or non-linear capacitance, the current flowing in it will be proportional to the capacitance value. It is usually set at 1 V/μsec. which gives 1 milliampere for 1 nano Farad.

Generally the drain-gate voltage is put on the x-axis and the different branch currents on y-axis.

For example:
- in **TMOSINIT.LIB, I(X1.CGDMAX)** or **I(X1.DGD)** represents C_{rss} (do not forget to give the right initial voltage value)
- in **TMOS.LIB**, C_{rss} is represented by **I(X1.CGDMAX)+I(X1.DGD)**
- and in both libraries:
  I(X1.DDS) is the Drain-Source Capacitance
  I(X1.CGS) is the Gate-Source Capacitance
  I(X1.RG) is the C_{iss} curve

5. **GATECHRG.CIR**

This gives you the gate charge versus gate-source voltage curve. This is another way to visualize your power

MOSFET capacitances: you charge the gate of the transistor with a constant current of 1 mA. For the load, a constant current source is used on the drain.

For a capacitance, the charge equations are: $Q = CV$ and $Q = it$

If i = Constant = 1 mA, 1 microsecond on the x-axis will be equivalent to 1 nanoCoulomb. Taking into account this unit change, the equivalent data sheet curve can be obtained.

6. **SWITCHING.CIR**

This is to check different switching characteristics, either inductive or resistive, clamped or not clamped (see Appendix).

IMPORTANT: users must be warned that the equivalent circuit of the inductive load has to be studied precisely before making any comparison between simulation and reality. Since power MOSFETs are very fast devices, sometimes the switching limitation can come from the inductance rather than the transistor itself. Poor quality inductances may have rather low resonance frequency which appears to be more capacitive than inductive at high frequency and high switching speed. Therefore, if poor correlation results please do not blame the TMOS library first, but check whether your equivalent inductance circuit is good by doing its Bode diagram.

7. **DGCLAMP.CIR**

This is a typical application for inductive switching. Instead of using an external power zener to do the clamp, a small signal zener is put between drain and gate. The TMOS power FET now dissipates the stored energy during the turn off rather than the power zener. It is very interesting to see the instantaneous power dissipated ($I_D V_{DS}$) into the TMOS device in this application. The peak power occurs during turn off. We noticed that the "ON" dissipation is negligible.

II. THE PHYSICS OF THE POWER MOSFET

Several suggestions for equivalent circuits have been recently published by International Rectifier, Motorola, RCA, University of Washington and other organizations. These models use two active components from the SPICE library which are the MOS and the JFET; the use of this JFET for the "quasi-saturation" phenomenon that was necessary to model the early high voltage devices in the market, is not necessary. Actual structures are optimized such that this phenomenon now appears only for drain currents well above the nominal current rating of the device.

This note describes a basic, but accurate, model for switching circuits with resistive and inductive loads. This model is compatible with the well known "SPICE" software. It works as well for low voltage structures (one hundred volts) of both standard and Logic Level (L^2FET with a nominal gate source voltage of 5 volts) types, with medium voltage (100–500 volts) and high voltage devices (>500 volts). Its configuration is based on a more complete but also more cumbersome to handle model whose parameters are all related to the physical properties and topology of the VDMOS transistor. Their values can be obtained from data sheets and some "classical" measurements. It must be pointed out that this model takes into account the high degree of non-linearity of the gate-drain and drain-source capacitors and also the short channel effects (variable mobility, saturation velocity, etc.) which mainly prevail in the low and medium voltage structures.

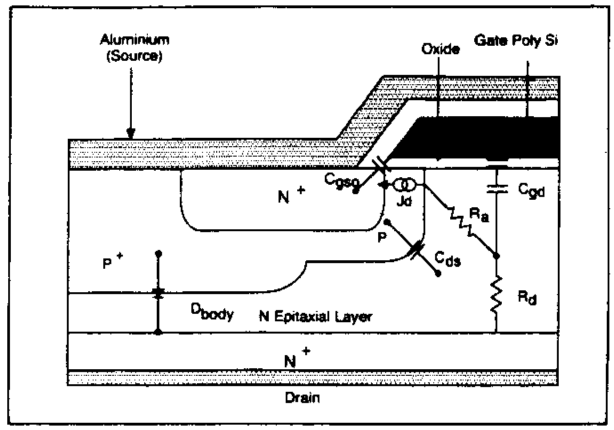

Figure 5. Cross Section of the VDMOS Transistor. Localization of the Simplified Model Elements.

The model structure is directly related to the power VDMOS geometrical topology (see Figure 5). We can notice on the schematic:

1. the intrinsic transistor (conduction channel) represented by the current generator J_d,
2. the n-type layer between the p wells with the access resistance R_a to the channel and the highly non-linear gate to drain capacitor C_{DG}, i.e. the depletion capacitor C_d in series with the thin gate oxide capacitor C_{GD}max,
3. the low doped n-type epitaxial bulk accounted for by the drift resistance R_d and the pn junction capacitor C_{DS} with the p well.

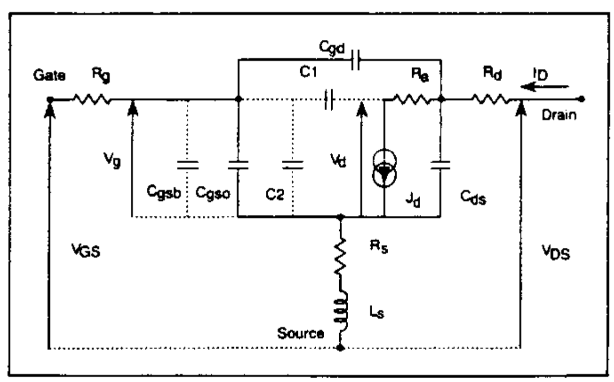

Figure 6. Simplified Model of the VDMOS Power Transistor in Conduction (in blocked mode, C_{gsb} is paralleled to C_{gso})

4. the gate metallization overlap of the N+ source diffusion which creates, through the thin and thick oxide, a constant parasitic capacitor C_{gso}.

When the MOS transistor goes through a switching phase, all the three different modes: blocked, ohmic and saturation are involved. The model (see Figure 6) takes into account these three operating modes.

The conduction channel under the gate, i.e. the intrinsic transistor, is described by the current generator J_d and the non linear capacitors C_1 and C_2.

In the "Ohmic" mode (i.e. $V_d < V_p$), the current J_d as approximated from the general formulation, is given by:

$$J_d = \frac{K_p\left((V_G-V_T)V_D - 0.5\,V_D^2\right)}{\left(1+(V_G-V_T)/psi\right)\left(1+V_D/LE_o\right)} \qquad (1)$$

with $K_p = \mu_o(W/L)C_{ox}$, where μ_o is the carrier mobility at low electric field level, W the channel perimeter, L the channel length, C_{ox} the gate oxide capacitor per unit area, V_g and V_d the gate-source and drain-source potentials, V_T the threshold voltage. "psi" and LE_o are the potentials related to the effect of the transverse and longitudinal electric fields on the carrier mobility in the channel (i.e. transverse roll-off limitation and longitudinal velocity saturation). Finally the capacitors C_1 and C_2 have the same value and are approximated to $(C_{ox}WL)/2$.

In the "Saturation" mode (i.e. $V_d \geq V_p$), the drain voltage V_p corresponding to the onset of the channel pinch-off, assuming a perfect current saturation i.e. there is no effect of channel length modulation, is given by:

$$V_p = LE_o\left(\left(1+2\,\frac{V_G-V_T}{LE_o}\right)^{1/2}-1\right) \qquad (2)$$

In this mode, the channel is pinched and "disappears" on the drain side, as does the capacitor C_1 and C_2 takes a value close to 2/3 $C_{ox}WL$.

In the "Blocked" mode (i.e. $V_G < V_T$), the drain current will theoretically be null as the "subthreshold" current is neglected, and the intrinsic transistor is reduced to one element: the oxide capacitor C_{gsb}. Although this is a distributed capacitor over the whole P region, for the model, it is assumed to be located between the gate and source electrodes.

$$C_{gsb} = C_{ox}WL \qquad (3)$$

The model is completed with the source inductance L_s which can induce an important feed-back effect from the output to the input.

The static parameter values K_p, V_T, psi, LE_o, R_a and R_d can be obtained from a specific approach with low and high level drain voltage measurements. The dynamic parameters R_g, C_1, C_2, C_{gso}, C_{gsb}, C_{GD}, C_{DS} and L_s, can be partially obtained with an original method developed previously, based on the constant current gate charge relationship.

III. IMPLEMENTATION OF THE MODEL FOR SPICE PROGRAMS

This VDMOS transistor model cannot be described by a single component of the SPICE library. Our approach is to build a macro-component (sub-circuit) in which each element (non-linear capacitor, current generator, etc.) is part of this model library. The current generator J_d, for example is represented by the MOS model level 3 or 1, and the non-linear C_{DS} and C_{GD} capacitors are represented by the transition capacitors of the diode model. The C_{GS} capacitor is constant as a first order approximation. Likewise, R_a and R_d (drift) resistors are constant. The macro model schematic for N-channels is shown in Figures 2 and 3. P-channel model has a similar schematic but some components are inverted. The listing of MTH5N100 and MTP3055E library is given in the Appendix. For the static characteristics, the "heart" is the current source J_d made with the small signal MOSFET model called M1. The drawing of its equivalent schematic is given Figure 7. Only the current source J_d of this model is used. The different MOS levels available are described below.

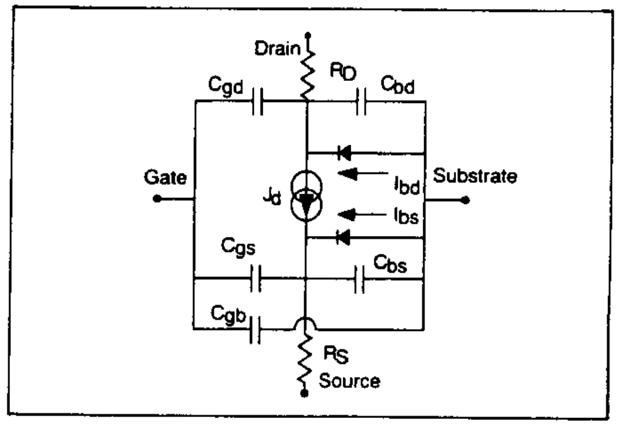

Figure 7. MOS Transistor Model Used in SPICE2G6

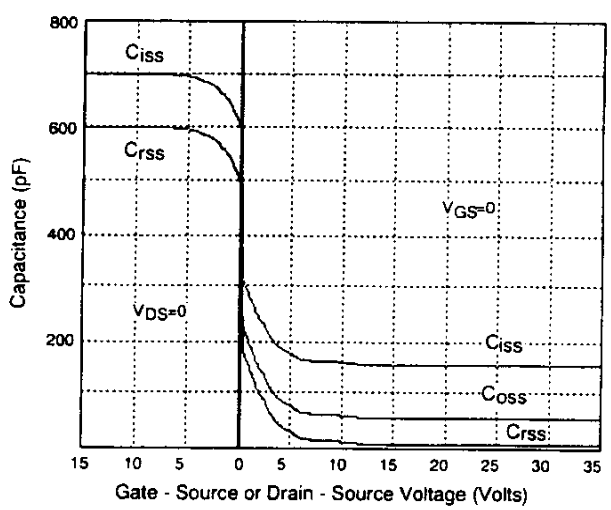

Figure 8. Capacitance Variation Curves versus Terminal Bias

In the dynamic mode the most important parameters are the MOS capacitances. Some are constant, some are non-linear. Figure 8 shows the capacitance variation curves given in the data sheets for a typical power MOSFET. The plateau can be simulated by a constant capacitor, and the non-linear part by the non-linear capacitance available in the SPICE diode model (called C_T in § II-2).

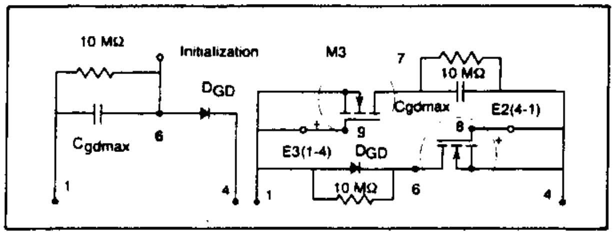

Figure 9. Models of the Capacitance C_{gd}

C_{GD} is the key of the model. Two solutions are described Figure 9. The diode (D_{GD}) uses the C_T capacitance. Added to the C_{GD} max capacitance, it gives the C_{rss} curve wished. In Figure 9a, these two components are in series. This requires an initialization step when doing a transient analysis to be sure to set up the proper voltage on node 6 at the beginning of the simulation. The model Figure 9b shows a heavier solution with more components, but which does not require this initialization step. One way to verify the capacitance modeling will be shown in Section V, with the well known gate charge curve.

C_{DS} is a pure transition capacitance. Therefore it will also be simulated by a diode (called D_{DS}).

C_{GS} is assumed to be constant in a first order approximation.

A. The SPICE MOSFET Model

SPICE 2G6 allows three different levels of equations for the MOSFETs. They are summarized in the following table:

Level	Drain Current in Ohmic Region	Relation
1	$J_d = \mu_o \frac{W}{L} C_{ox}[(V_G-V_T)V_D - \frac{V_D^2}{2}]$	(4)
2	$J_d = \mu_S \frac{W}{L} C_{ox}\{[(V_G-V_{bin} - \frac{hV_D}{2}] - \frac{2}{3}gS\,[(2jF+V_D)^{3/2} - (2jF)^{3/2}]\}$	(5)
3	$J_d = \mu_{eff} \frac{W}{L} C_{ox}[(V_G-V_T)V_D - (1 + F_B)\frac{V_D^2}{2}]$	(6)

Level 1 corresponds to a classical model for long channel MOSFETs. It is the simplest one and can be used for high voltage TMOS devices which have a long channel behavior.

Level 2 takes into account the short channel effect of the MOSFETs. The mobility μs is given as follows:

$$\mu s = \mu_o \left[\frac{U_{CRIT}\,\epsilon_o \epsilon_{si}}{C_{ox}\,[V_G-V_T-U_{TRA} \cdot V_d]}\right]^{Uexp} \quad (7)$$

It has not been retained for our library mainly because of its complexity which was in contradiction with our objectives.

Level 3 is a somewhat similar to level 1, but takes into account the mobility modulation. We have:

$$\mu_{eff} = \frac{\mu_s}{1 + \left[\frac{\mu s\, V_D}{V_{max} L}\right]} \quad (8)$$

In this equation, V_{max} represents the maximum drift velocity of channel carriers (V_{max} is equivalent to $\mu_o E_o$ in equation (1)). μ_s is the surface mobility in the channel inverted layer. It is dependant of the transverse electric field, following the equation:

$$\mu_s = \frac{\mu_o}{1 + \Theta(V_G-V_T)} \quad (9)$$

where μ_o is the mobility at low level field, Q a parameter which takes into account the influence of the transverse field over the carrier mobility (Q = 1/psi, the psi of the equation (1)).

Level 3 is, the best model available in SPICE to simulate the current source J_d for low and medium voltage TMOS devices which tend to have a short channel behavior. It is also very effective for logic level power MOSFETs with thin gate oxide which depend more on the transverse field.

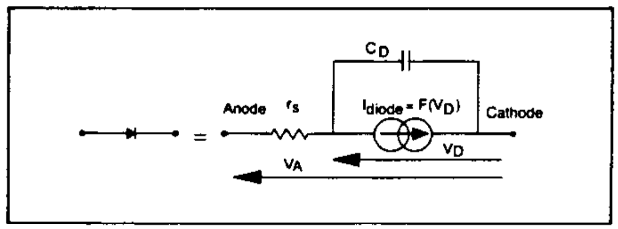

Figure 10. Diode Model Used in SPICE2G6

B. The SPICE Diode Model

The equivalent schematic is described Figure 10. The static equation is given as follow:

$$I_{diode} = I_s\left[\exp\left[\frac{V_D}{nU_T}\right] - 1\right] \quad (10)$$

I_s represents the saturation current.
V_D the voltage across the junction.
n the ideality factor, also called emission coefficient.
U_T = KT/q the thermodynamic voltage.

The dynamic behavior is what we need for our capacitance modelization:

$$C_D = \frac{tauI_s}{nU_T} \cdot \exp\left(\frac{V_D}{nU_T}\right) + \frac{C_{jo}}{\left[1 - \frac{V_D}{F_{DB}}\right]^m} \quad (11)$$

The first part is directly proportional to the transit time tau (TT in SPICE) of the minority carriers. It is the storage capacitance (C_S).

The second part represents the transition capacitor (C_T).

"m" is the grading coefficient of the PN junction. Its value is within 0.3 and 0.5 for a real junction.

"FDB" (called V_J in SPICE) is the junction diffusion potential.

C. The Body Diode

In order to differentiate the capacitance effect C_{DS} from the internal drain-source diode, an extra component called D_{BODY} is added to simulate the behaviour. Fortunately the SPICE diode model is sufficient and no extra components like the TMOS devices are needed. The related equations are 10 and 11 as described above. The C_S part is used to simulate the storage time. The capacitance, C_T is not used.

IV. PARAMETER EXTRACTION METHOD

We shall split the study in three parts:

1. The parameters needed for the static characteristics
2. The parameters needed in the dynamic mode for the transient analysis
3. The parameters needed for the body diode.

A. Parameters for the Static Characteristics

As explained in the previous chapter, the low and medium voltage devices require level 3 of the SPICE MOSFET model to fully simulate the power MOSFET. On the other hand, the high voltage power MOSFETs can accommodate model level 1 as well as level 3.

1. Basic Considerations

As precise data on the technological process of the products are not available to the end users, some assumptions are made:

a) For convenience, the channel parameters W,L, are given the value 1 μm. Then K_p represents the effective transconductance: $K_p = (\mu_o C_{ox}) . W_{effective}/L_{effective}$

b) The source resistance R_s is primarly due to the bonding wire and the metalization/diffusion layers of the chip. In actual products, R_s is negligible when compared to the others resistances, one milli Ohm is attributed to this parameter in all the products.

c) Looking at R_a, R_d, the split is done with a rule of thumb as follow:

For (50 V–100 V) power MOSFET: $R_a = R_{dson}/3$
For (100 V–500 V) power MOSFET: $R_a = R_{dson}/5$
For (500 V–1000 V) power MOSFET: $R_a = R_{dson}/10$

2. MOSFETS Using Model Level 1
(High voltage products only)

The parameters to be extracted are K_p, V_T, R_a and R_d.

K_p, V_T: the method involves the classical transfer characteristic of the data sheet at a given drain bias i.e. V_{DS} = 10 V. As the device is working in the saturation region, the current is given by:

$$I_{dsat} = \frac{K_p}{2} \frac{W}{L} (V_{GS}-V_T)^2 \text{ for } V_{DS} \geq V_{GS}-V_T \quad (12)$$

and the parameters are obtained from $I_{dsat}^{0.5}$ versus V_{GS} characteristic as shown in Figure 11.

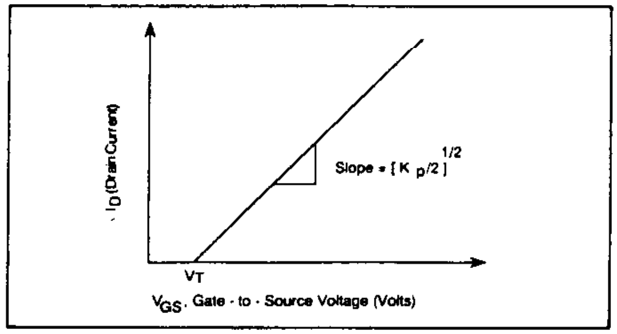

Figure 11. Determination of the Conductance K_p and Threshold Voltage V_T for the Level 1 Model

R_a, R_d: they are related to the static drain-source on-resistance as defined in the data sheet accordingly to equation 4 and the following relationship:

$$R_{DS(on)} = R_a + R_d + V_D/J_d \quad (13)$$

The static model using level 1 is now complete. It is written in SPICE language as follows:

```
M1 2 1 3 3 DMOS L=1U W=1U
.MODEL DMOS NMOS (VTO=xxx KP=xxx LEVEL=1)
RA 2 4 xxx
RD 4 20 xxx
```

In order to verify it, the ONCHARAC.CIR and TRANSCAR.CIR files will help you to generate the two important curves for the static characteristics:

— ON-Region characteristics curve
— Transfer characteristic curve

Some adjustments of K_p and V_T may be needed for an exact fit between simulation and the reference curves.

3. MOSFETS Using Model Level 3
(medium and low voltage products)

The related equations are (6)-(9) and the parameters to be extracted: K_p, V_T, F_b, V_{max}, Theta, R_a, and R_d.

F_b is related to the channel length L modulation due to the extension of the junction space charge in the channel substrate. Since power MOSFETs, due to the low doped drain, present a perfect current saturation, F_b must be taken as zero (default value).

Theta is proportional to the reciprocal of gate oxide thickness:

For a 1000 Angströms device (standard)
Theta = 0.04
For a 500 Angströms device (L^2FET)
Theta = 0.08

K_p, V_T, R_a and R_d: the method involves the current-voltage relationship in the ohmic mode, at low level drain bias, e.g. $V_{DS} \leq 10$ mV. Then, along with the relationship between intrinsic and extrinsic drain bias, i.e. $V_d = V_{DS} - (R_a + R_d)I_d$, equations 6–9 will give:

$$R_{DS(on)}(V_{GS}-V_T) = 1/K_p + (V_{GS}-V_T)^* \left(\frac{\Theta}{K_p} + R_a + R_d\right) \text{ for } V_{DS} \rightarrow 0 \quad (14)$$

Further, at gate bias near the threshold voltage, equation 6 will reduce to:

$$I_d = K_p(V_{GS}-V_T)V_{DS} \text{ for } V_{DS}, (V_{GS}-V_T) \rightarrow 0 \quad (15)$$

The determination of K_p and V_T, in accordance with the above equation, is obvious as shown in Figure 12.

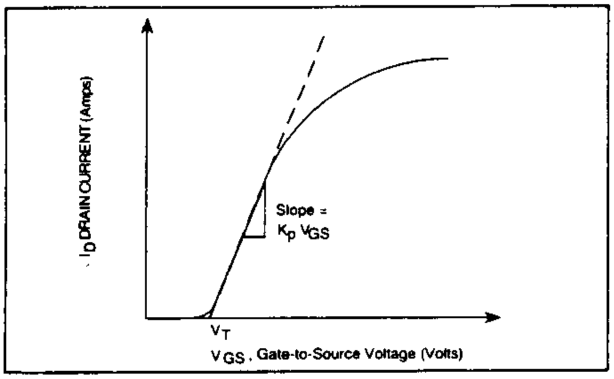

Figure 12. Determination of the Conductance K_p and the Threshold Voltage V_T for the MOSFET Level 3

Finally, the resistances are obtained from the slope of the curve 13 according to relation 14.

V_{max}: the maximum drift velocity is used to adjust the saturation level of the drain current versus the gate bias. Its value is within xxx and xxx.

The model using level 3 is now completed. It is written in SPICE as follows:

```
M1 2 1 3 3 DMOS L=1U W=1U
.MODEL DMOS NMOS (VTO=xxx KP=xxx
  THETA=xxx VMAX=xxx LEVEL=3)
RA 2 4 xxx
RD 4 20 xxx
```

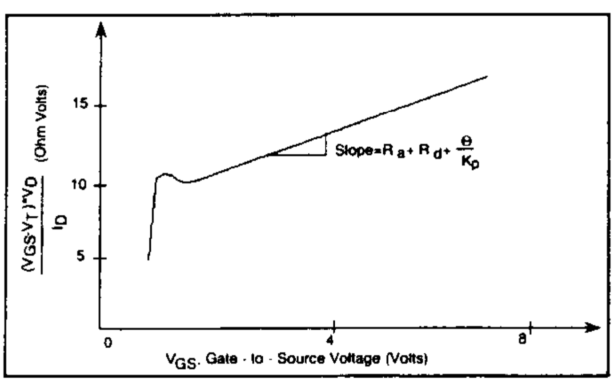

Figure 13. Determination of the Series Resistances $R_a + R_d$ for the MOSFET Level 3 Model

Verification can be done with ONCHARAC.CIR and TRANSCAR.CIR files too.

B. Parameters for The Dynamic Characteristics

The related parameters are: C_{GS} (gate-source capacitor), C_{DDS} (drain-source capacitor simulated by a diode), C_{GDmax} and C_{DGD} (drain-gate Capacitors), L_s and R_g.

1. Ls

This parameter takes into account the parasitic inductance inside the package, primarily the bonding wire. At very fast switching it may be very important, and must be taken into account. The value attributed to it depends on the package as follow:

TO-204 (TO-3) (metal): 10 nano Henry
TO-220 (plastic): 5 nano Henry
TO-218 (plastic): 8 nano Henry (for one wire on source pad)
4 nano Henry (for two wires)

2. The Capacitances

When it is available, the document of reference for these parameters is the data sheet curve called "Capacitance Variation", but of course, another way is to measure these values on the component itself by using a bench setup if available (for example HP or BOONTON 72-B). It is important to have both positive and also negative bias curve in order to have an accurate dynamic model.

We faced some difficulties when simulating these capacitances. SPICE2G6 allows polynomial equations. This could have been acceptable for the low voltage products, which have a rather symmetrical capacitance variation curve and could fit with a power eight polynom, but not good at all for the high voltage ones. Therefore, for a question of homogeneity, the non-linear capacitor of the diode model available in SPICE, is used.

In the diode model (Figure 9 and relation 11), the capacitance is given as:

$C_D = C_S + C_T$
! !
! Transition capacitor
Storage capacitor

The storage capacitor is not critical for us to simulate the TMOS device capacitances. On the other hand, the transition capacitor is exactly the one needed: a non-linear capacitance.

The capacitances which can be measured (or given by the datasheets, see Figure 8) are:

$$\begin{aligned} Ciss &= C_{GS} + C_{GD} \\ C_{oss} &= C_{GD} + C_{DS} \\ C_{rss} &= C_{GD} \end{aligned} \quad (16)$$

Let us get the value of C_{DS}, C_{GD} and C_{GS}:

a. C_{DS}:

From the above equations: $C_{DS} = C_{oss} - C_{rss}$. It is considered as a pure transition capacitance. According

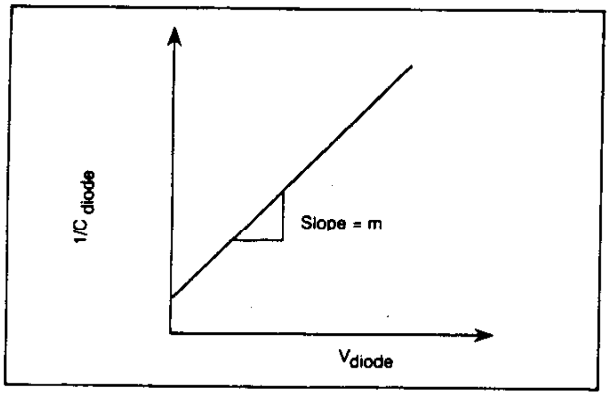

Figure 14. Typical Variation of $1/C_{diode}$ Function of V_{diode} (Log-Log Diagram). Determination of the Grading Coefficient m.

to expression 17 of relation 11, the parameters m and C_{jo} can be extracted from the $1/C_{DS}$ versus drain-source voltage curve on a Log/Log diagram as shown on Figure 14:

$$m\mathrm{Log}(1 - V_{DS}/V_j) = \mathrm{Log}(C_{jo}/C_{DS}) \qquad (17)$$

m represents the slope of this linear curve.
C_{jo} is the capacitance at $V_{DS} = 0$.
V_j is obtained for an arbitrary voltage value of V_{DS} with the equation:

$$V_j = V_{DS}/((C_{jo}/C_{DS})^{1/m} - 1) \qquad (18)$$

b. C_{GD}:
The C_{GD} capacitance is a mix of a constant capacitor (C_{GD}max) and a non linear capacitor built with the transition capacitor of a diode (D_{GD}) in reverse bias.
The upper plateau of C_{rss} in the Capacitance Variation Curve of the data sheet (see Figure 8) directly gives C_{GD}max. This will build the plateau of the negative bias side of the capacitance model.
About the parameters of D_{GD}, we shall distinguish two cases:

a) C_{GD} in TMOS.LIB
The two elements are in parallel and are alternately switched on with the help of the switches named M2 and M3. The parameters for D_{GD} are obtained as for the determination of C_{DS}. With the assumption $C_{jo} = C_{GD}$max, the parameter m is extracted graphically from the ($V_{GS} = 0$) part of Crss versus V_{DS} according to the following relation:

$$m\mathrm{Log}(1 - V_{DS}/V_j) = \mathrm{Log}(C_{jo}/C_{rss}) \qquad (19)$$

V_j is obtained for an arbitrary voltage value of V_{DS} with the equation:

$$V_j = V_D/((C_{jo}/C_{rss})^{1/m} - 1) \qquad (20)$$

b. C_{GD} in **TMOSINIT.LIB**
It is slightly different since, as shown on Figure 15, the two "capacitors" are now in series:

$$1/C_{rss} = 1/C_{GD}\mathrm{max} + 1/C_{(DGD)} \qquad (21)$$

The part of the potential drop across $C_{(DGD)}$ is given by:

$$V_1 = V_{DS}\{1 - 2C_{(DGD)}/C_{GD}\mathrm{max}\} \qquad (22)$$

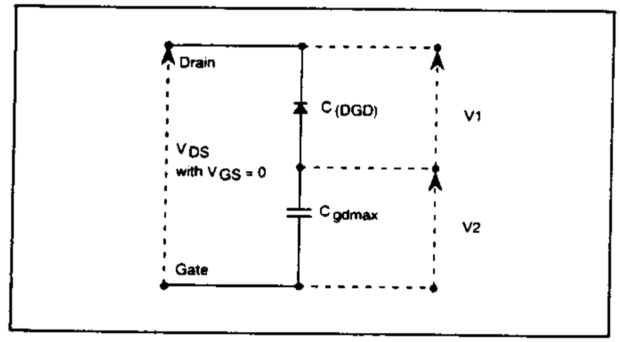

Figure 15. Drain-Gate Capacitance Representation

According to the above relations, a table of the values of $C_{(DGD)}$ with the associated potential V_1 must be calculated from the C_{rss} versus V_{DS} characteristic. Then the parameters m, C_{jo} and V_j for $C_{(DGD)}$ are determined as for the C_{ds} case.

c. C_{GS}

$$C_{GS} = C_{iss} - C_{rss} \qquad (23)$$

An average value of C_{GS} can be extracted from the capacitance variation curves (Figure 8).
Another way is to take the first slope of the gate charge curve. Its slope is $D(V_{GS})/D(Q)$, equivalent to C_{iss}, that is to say, C_{GS} in parallel with C_{GD}.
All these capacitance curves can be checked afterwards with the **CAPACITY.CIR** program detailed on page 4.

3. R_G:
This is the last parameter of the group. Gate access resistance should be very low, but sometimes it is not that low. As seen mainly through the resistive switching, putting zero to this parameter will affect the delay times, especially when the transistor is driven by a very low impedance circuit. Since this gate access resistance is spread all over the chip, it is hard to be calculated. The way to solve that problem is to do a resistive switching on your bench and compare with the value given with **RESISTSW.CIR** program and fit R_G to the proper value in order to get a good match on the delay times.

C. Parameters for the Body Diode
The power MOSFET has an intrinsic diode which needs to be modeled for some applications such as H-bridge circuits.

The full SPICE diode model is described in § II-2. As the transition capacitance is already accounted for by C_{DS}, the only dynamic parameter to be considered is the transit time tau. Thus, the parameters to be extracted are n, I_S, r_S, tau

n, I_S: accordingly to equation 10, the current as a function of the direct bias, is given by:

$$\mathrm{Log}\left(\frac{I_{diode}}{I_S}\right) = \frac{1}{nUT} \cdot (V_D - r_S I_{diode}) \qquad (24)$$

At low current level, i.e. some tenths of ampere, the parasitic drop $r_S \cdot I_{diode}$ can be neglected. Then the parameters n (the slope-1) and I_S (the extrapolated value at V_D = 0) can be extracted from the linearized variation of $\mathrm{Log}(I_{diode})$ versus the drain-source bias.

r_S: at a second step, at high current level in the range of the rated drain value, equation 24 will give the value of the series resistance.

tau: a realistic value of the transit time is obtained from the injected charge Q_{rr} during the reverse recovery test:

$$Q_{rr} = I_{RM} \cdot \mathrm{tau} \qquad (25)$$

BV: The reverse breakdown voltage value must be the one guaranteed in the data sheet. For a 60 volts product, it should be 60 volts, even if the measured value is higher.

I_{BV}: The reverse breakdown current is related to BV as follows:

$$I_{breakdown} = I_{BV} \cdot \exp\left(\frac{-BV - V_D}{UT}\right) \qquad (26)$$

Specific measurements must be carried out prior to the determination of I_{BV}.

The resulting general form is:

DBODY 3 20 DBODY
.MODEL DBODY D(IS = 1.1E − 11 N = 1.03 RS = 0.050 TT = 200N BV = 60 IBV = xxx)

V. THE RESULTS: SIMULATION versus MEASUREMENTS

The best proof that our model works well is to try it on your own application. In order to demonstrate how accurate it is, some typical results are given here.

A. The ON Characteristics

It is a pure static test which gives the current for a given drain-source and gate-source voltage. Figure 16 describes both simulation (fine trace) and the measurement (thick grey trace) of one production part, the MTP3055E, which is typical of the production line.

A good fit can be noticed. For products not centered on the normal curve, a 10 to 20% difference has be seen. The curve at V_{GS} = 10 V is very dependent on the $R_{ds(on)}$ of the product. Because of the steep slope, a difference can be seen in the figure.

B. The Gate Charge Curves

It is available in the data sheets but again has to be used with care as well. This test gives the gate-source voltage curve when the gate is driven with a constant current of 1 mA.

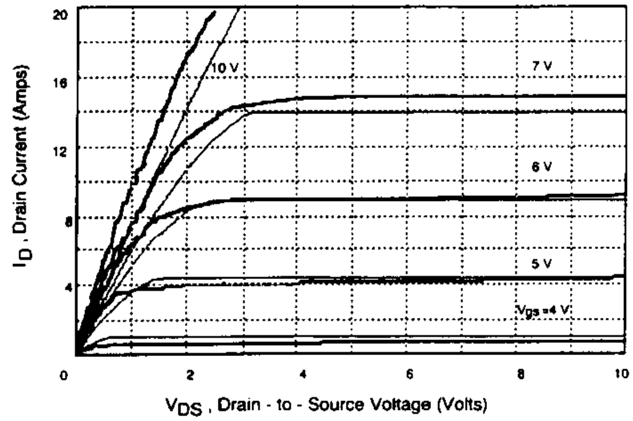

Figure 16. ON Region Characteristics for MTP3055E
Measurement: Thick trace
Simulation: Fine trace

The first part of the curve corresponds to the charge of the C_{iss} capacitance. When the threshold is reached (for a given I_D) we get a plateau where length is related to the C_{rss} Miller value. After charging this Miller capacitance, we again have the voltage rise of C_{iss}. Figure 17 gives both simulation and bench measurement curves for MTH40N06. The slopes have 10% difference for the products the furthest away from the mean value.

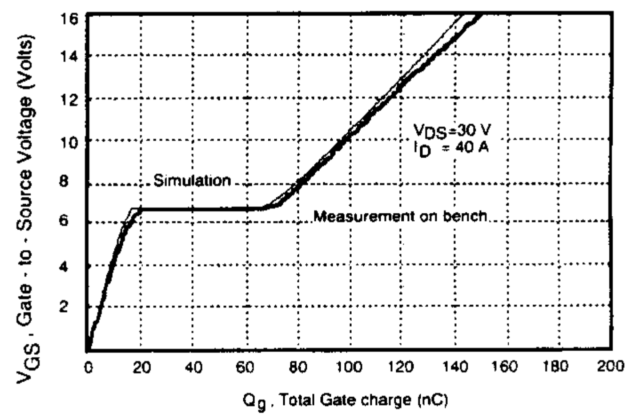

Figure 17. Gate Charge Characteristics for MTH40N06
Simulation: Fine trace
Measurement: Thick trace

C. The Inductive Switching Tests

In order to verify the model in dynamic mode, one of the best solutions is to use it in an inductive switching configuration. SPICE allows transient analysis and the two kind of tests which are described here:

1. A clamped inductive test where the active clamp stands between drain and gate
2. An unclamped inductive switching (U.I.S.) test to test the dynamic resonance of the circuit.

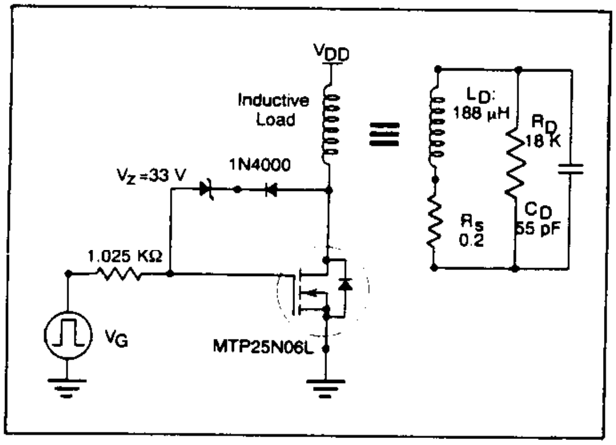

Figure 18. Inductive Switching with Drain-Gate Active Clamp

1. The Drain Gate Clamped Inductive Switching Test:

Instead of using a drain-to-source power zener to do the clamping at turn off, we use the power transistor as a power zener. The principle is very basic: As soon as the clamping voltage is reached during turn off, the transistor is turned on again until all the energy has been dissipated into the switch. The typical schematic is given in Figure 18.

One of the key points when working with simulation programs is to know the characteristics of all the components. This is already true for the power MOSFET library which retained all our attention, but the users have to introduce the equivalent schematic of the inductive load. Therefore an equivalent schematic of the coil studied has been built. It is described on the right part of Figure 18.

It is easy to notice that at very high switching speed, the coil will behave much more like a capacitance rather than as an inductance. This means a different stress for the component.

Figure 19 shows the simulation waveform and should be compared with the oscillogram of the real measurement.

The drain current, the drain-source and gate-source voltage and also the instantaneous power dissipation are given. It can be noticed easily that most of the power dissipated by the transistor occurs during turn off. The

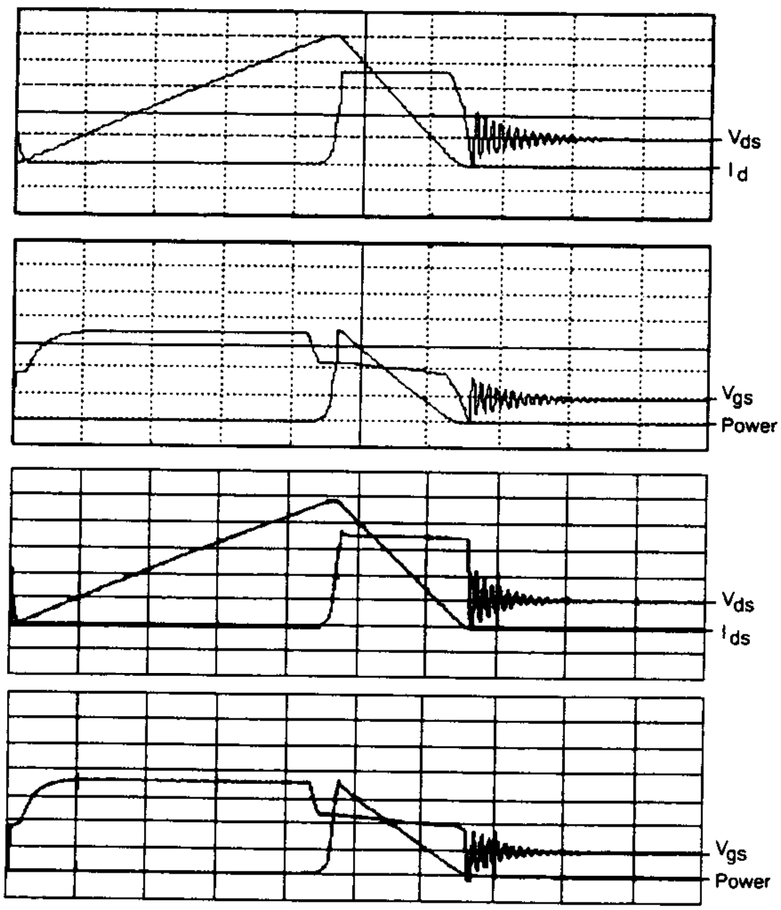

Figure 19. Drain-Gate Clamped Inductive Switching with MTP25N06L:
V_{DS} = 10 V/div, I_D = 5 A/div, V_{GS} = 2 V/div, Power = 50 W/div, Time = 20 µs/div
Simulation (top) — Measurement on Bench (Bottom)

precision of the simulation is in the range of 10% at 25°C. With a closer look at the gate source voltage, we also notice that the power device works in linear all along the turn off time, until the energy is dissipated. The V_{GS} plateau is in the range of 2 V which is the threshold voltage of the logic level TMOS MTP25N06L.

The gate voltage waveform allows observing the type of stress on the logic. Here, of course, the application is safe and no damaging over-voltage was seen on the logic. Some simulations performed on other applications show phenomenon which were difficult to see with an oscilloscope.

2. The Unclamped Inductive Switching (U.I.S.) Test

This test becomes very significant since power MOSFETs of the E-series (Energy) can now withstand

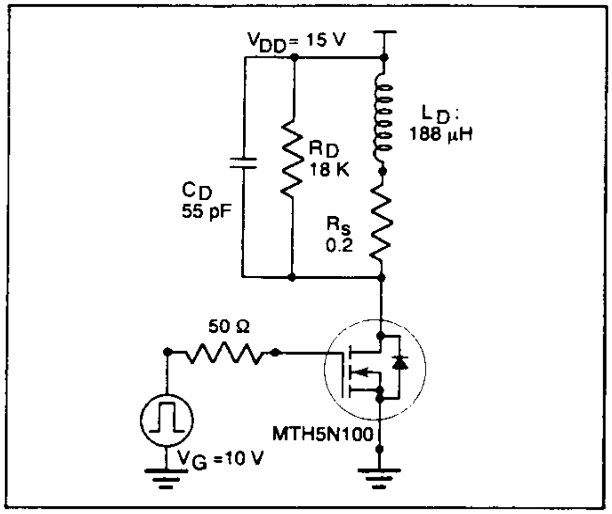

Figure 20. Unclamped Inductive Switching with MTH5N100:

the avalanche. Our goal was not to avalanche the MTH5N100 in the test configuration shown in Figure 21, but to check the over-voltage value at turn off when the circuit is supplied with a low voltage ($V_D = 15$ V).

This over-voltage described in Figure 22 depends very much on the impedance of the whole circuit. Good knowledge of the load characteristics and of the circuit parasitic inductances would make the simulation more accurate, however, it can be seen here that even with our simple inductance model, adequate simulation waveform is achieved.

CONCLUSION

In conjunction with the knowledge of the solid state physics of power MOSFETs and the electric modelization, a rather basic model has been developed which works in both static and dynamic mode. We are now able to simulate the power MOSFET and determine its instantaneous power consumption, whether the losses are in the ON state or during switching.

One interesting point for future consideration will be to establish the effect of the increase in die temperature

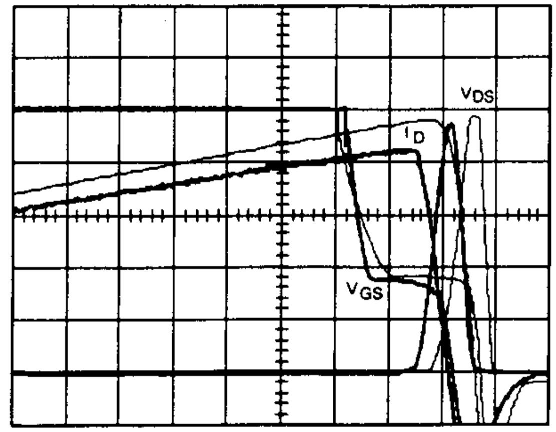

Figure 21. Unclamped Inductive Switching with MTH5N100:
V_{DS} = 100 V/div, I_D = 200 mA/div, V_{GS} = 10 V/div, Time = 500 ns/div
Simulation: Fine trace
Measurement: Thick trace

of the power MOSFET and re-inject this data into the transistor model. This is a more complicated study which will require additional time. Another interesting idea is to do the same type of work on bipolar power transistors. The Gummel-Poon model already exists in the SPICE2G6 program but does not fully simulate the non-linearity of this type of power product. An approach similar to that used for TMOS power MOSFETs may be needed.

As noticed here, there were many elements yet to be done for power transistors, and since technology is advancing toward combining more logic with the power control elements in the same package (Hybrid) or on the same chip (smart power) such simulation models will be an invaluable tool for the future designs.

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GLOSSARY

BV:	Reverse breakdown voltage
C_{jo}:	Zero bias junction capacitance in spice diode model
C_{ox}:	Oxide capacitance
C_s:	Storage Capacitor
C_T:	Transition Capacitor
$F_{db} = V_J$:	Diffusion Potential
I_S:	Saturation Current
K_p:	Transconductance parameter
level:	Model index
L_s:	Source wire inductance
m:	Grading coefficient
n:	Emission coefficient
$\theta = 1/\text{psi}$:	Mobility modulation
Q_{rr}:	Storage charges in a diode
R_a:	Access resistor of the TMOS model
R_d:	Drift resistor of the TMOS model
R_s:	Source wire resistance in TMOS model
Tau = TT:	Transit time
U_T:	Thermodynamic Voltage
V_D:	Voltage across junction
V_{DS}:	Drain Source Voltage
V_{GS}:	Gate Source Voltage
V_j:	Junction potential
VT_o:	Zero Bias threshold voltage
μ_o:	Mobility at low level field

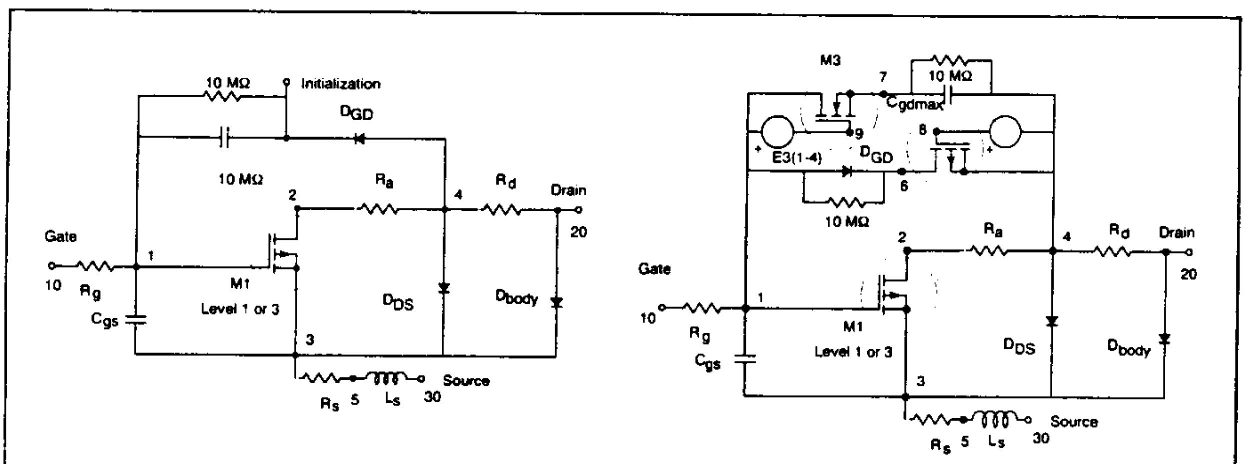
— APPENDIX —
LIBRARY OF THE TMOS SPICE MODELS

N-Channel TMOS

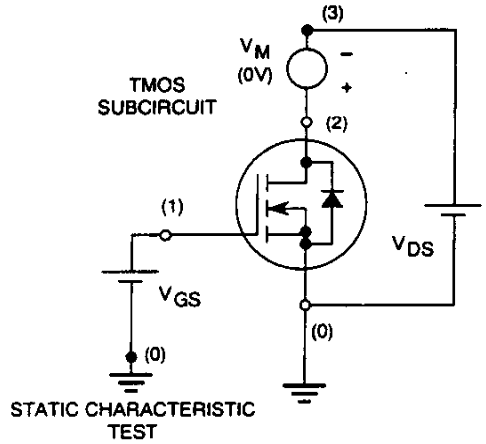
MTP3055E	MTH30N20	MTP4N85
MTP15N06E	MTM15N40	MTP3N100
MTP25N06L	MTP4N50	MTH5N100
MTP25N06	MTH13N50	
IRF541	MTP6N60	
MTP35N06E	MTM8N60	
MTH40N06	MTH8N60	

P-Channel TMOS

MTP12P10
MTP2P50



Appendix 1. Description of the P-Channel Models



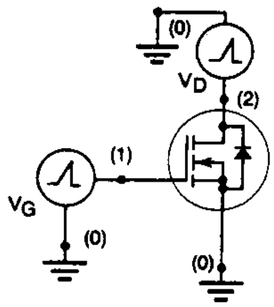

```
ON-REGION CHARACTERISTICS OF MTP3055E
PROGRAM — ONCHARAC.CIR
VD 3 0
VMTP3055E 3 2
VG 1 0

  TO BE USED WITH THE FASTER MODEL
X1 2 1 0 8 MTP3055E
.LIB TMOSINIT.LIB

X1 2 1 0 MTP3055E
.LIB TMOS.LIB

.DC VD 0 20 0.2 VG 4 10 1
.PROBE I(VMTP3055E)
.END
```

Testbox. On-Region Characteristics Circuit

```
ID=F(VGS) FOR MTP15N06E
  PROGRAM ID-VGS.CIR
    ADJUST VD TO THE SPEC
VD 3 0 10
VMTP15N06E 3 2 0
VG 1 0

    TO BE USED WITH THE FASTER MODEL
X1 2 1 0 8 MTP15N06E
.LIB TMOSINIT.LIB

X1 2 1 0 MTP15N06E
.LIB TMOS.LIB

.IC V(1)=0
.DC VG 0 10 .2
.PROBE I(VMTP15N06E)
.END
```

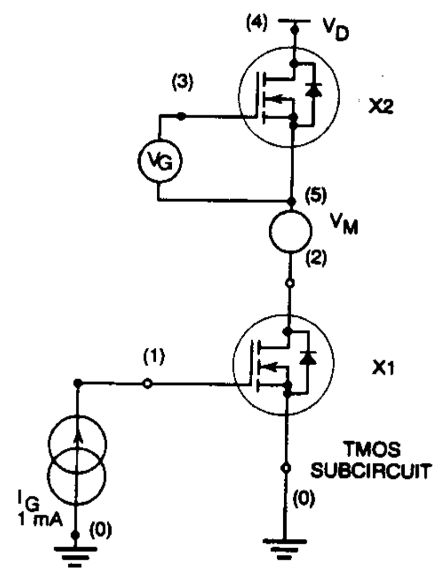
```
RDSON CHARACTERISTIC OF MTP3055E
  PROGRAM RDSON.CIR
    ADJUST ID & VG TO THE SPEC
ID 0 3
VMTP3055E 3 2
VG 1 0 DC 10
    TO BE USED WITH THE FASTER MODEL
X1 2 1 0 8 MTP3055E
.LIB TMOSINIT.LIB

X1 2 1 0 MTP3055E
.LIB TMOS.LIB

.DC ID .1 25 .1
.PROBE V(2) I(VMTP3055E)
.OPTION TNOM=27
.END
```

Testbox. I_D-V_{GS} and $r_{DS(on)}$ Characteristics Circuit




```
CAPACITY TEST OF MTP15N06E
     CAPACITY.CIR PROGRAM
VD 2 0 PULSE(50 0 0U 50U 0U 100U 101U)
VG 1 0 PULSE(0 20 50U 20U 0U 100U 100U)

     TO BE USED WITH THE FASTER MODEL
  BUT YOU NEED TO SET UP V(8) PROPERLY
X1 2 1 0 8 MTP15N06E
.IC V(1)=0 V(8)=4.041
.LIB TMOSINIT.LIB

X1 2 1 0 MTP15N06E
.IC V(1)=0
.LIB TMOS.LIB

.TRAN 10N 70U 0N
.PROBE V(2,1) I(X1.CGDMAX) I(X1.DGD)
+I(X1.DDS) I(X1.CGS) I(X1.RG)
.END
```

Testbox. Capacity Test Circuit

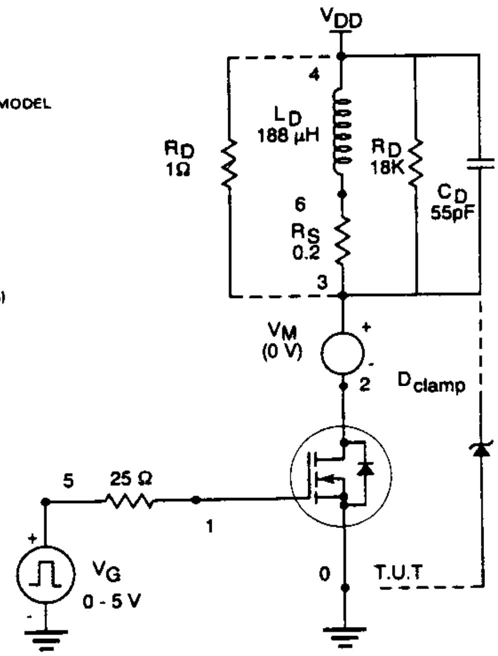



```
GATE CHARGE TEST OF MTH40N06
  GATECHRG.CIR PROGRAM
    ADJUST BV & ID ----
VD 4 0 DC 30
VMTH40N06 5 2
VG 3 5 DC 7
IG 0 1 PULSE(0 1M 0U 10N 10N
+200U 205U)

   TO BE USED WITH FASTER MODEL
X1 2 1 0 8 MTH40N06
X2 4 3 5 9 MTH40N06
IC V(1)=0 V(8)=2 v(9)=30
LIB TMOSINIT.LIB

X1 2 1 0 MTH40N06
X2 4 3 5 MTH40N06
.IC V(1)=0 V(2)=30
.LIB TMOS.LIB

  TSTEP, TSTOP,TSTART,TMAX
.TRAN 10N 200U 0N
.PROBE V(2) V(1) I(VMTH40N06)
.OPTIONS ITL4=40 ITL5=0
+RELTOL=0.01
.END
```

Testbox. Gate Charge Test Circuit

```
SWITCH OF MTP25N06
  SWITCHNG.CIR PROGRAM
    EQUIVALENT Inductive Load
LD 4 6 188U
RS 6 3 .2
CD 4 3 55PF
RD 4 3 18K
  RESISTIVE LOAD (OPT.)
RD 4 3 1
  DRAIN SOURCE CLAMP (OPT.)
DCLAMP 0 3 DCLAMP
.MODEL DCLAMP D(BV=40 RS=1)
```

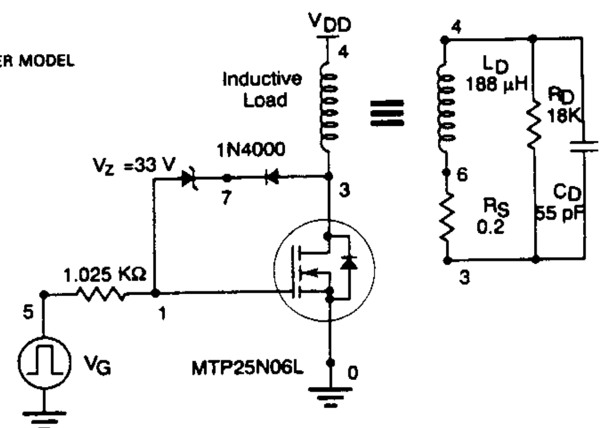
```
VDD 4 0 DC 3
VMTP25N06 3 2
RG 1 5 25
  TO BE USED WITH FASTER MODEL
X1 2 1 0 8 MTP25N06
.IC V(8)=2 V(1)=0
.LIB TMOSINIT.LIB

X1 2 1 0 MTP25N06
.LIB TMOS.LIB
VG 5 0 PULSE(0 10 2U 10N
+10N 4.6U 20U)
.TRAN 10N 20U 0 40N
.PROBE V(1) V(2) I(VMTP25N06)
.END
```



Testbox. Switching Test Circuit

```
IND. SW. CLAMP D-G MTP25N06L
  DGCLAMP.CIR PROGRAM
    REAL inductive load
LD 4 6 188U
RS 6 3 0.2
CD 4 3 55PF
RD 4 3 18K
  DRAIN GATE CLAMP
LZ 9 3 1N
DCLAMP 1 7 ZENER
DSERIE 3 7 DIODE
.MODEL ZENER D(BV=33 RS=1
+TT=10N IBV=1E-12)
.MODEL DIODE D(BV=70
+IBV=1E-12)
```

```
VDD 4 0 DC 12
VMTP25N06L 9 2
RG 1 5 1.025K

  TO BE USED WITH FASTER MODEL
X1 2 1 0 8 MTP25N06L
.IC V(8)=2.58
.LIB TMOSINIT.LIB

X1 2 1 0 MTP25N06L
.LIB TMOS.LIB
VG 5 0 PULSE(0 5 0U 10N
+10N 1.3m 2.5m)
.TRAN 10N 2m 0
.PROBE
.END
```



Testbox. D-G Clamp Test Circuit

EXAMPLES OF THE LIBRARY TMOS.LIB

```
.SUBCKT MTP3055E 20 10 30
RG 10 1 10
M1 2 1 3 3 DMOS L=1U W=1U
.MODEL DMOS NMOS (VTO=3.32 KP=5.5
+THETA=0.058 VMAX=1.5E5 LEVEL=3)
CGS 1 3 300P
RD 20 4 0.078
DDS 3 4 DDS
.MODEL DDS D(BV=60 M=0.42 CJO=600P
VJ=0.60)
DBODY 3 20 DBODY
.MODEL DBODY D(IS=1.1E-11 N=1.03 RS=0.050
+TT=200N)
RA 4 2 1E-3
RS 3 5 1M
LS 5 30 5N
M2 1 8 6 6 INTER
E2 8 6 4 1 2
.MODEL INTER NMOS (VTO=0 KP=10
LEVEL=1)
CGDMAX 7 4 605P
RCGD 7 4 1E7
DGD 6 4 DGD
RDGD 4 6 1E7
.MODEL DGD D(M=0.53 CJO=605P VJ=0.08)
M3 7 9 1 1 INTER
E3 9 1 4 1 -2
.ENDS
*
*        END OF SUBCIRCUIT
```

```
.SUBCKT MTH5N100 20 10 30
RG 10 1 5
M1 2 1 3 3 DMOS L=1U W=1U
.MODEL DMOS NMOS (VTO=3.36 KP=3.73
LEVEL=1)
CGS 1 3 1642P
RD 20 4 1.50
DDS 3 4 DDS
.MODEL DDS D(BV=1000 M=0.48 CJO=873P
VJ=0.43)
DBODY 3 20 DBODY
.MODEL DBODY D(IS=3.6E-11 N=1.03 RS=0.057
+TT=1U)
RA 4 2 1E-3
RS 3 5 1M
LS 5 30 8N
M2 1 8 6 6 INTER
E2 8 6 4 1 2
.MODEL INTER NMOS (VTO=0 KP=10
LEVEL=1)
CGDMAX 7 4 7500P
RCGD 7 4 1E7
DGD 6 4 DGD
RDGD 4 6 1E7
.MODEL DGD D(M=0.5 CJO=7500P VJ=0.00337)
M3 7 9 1 1 INTER
E3 9 1 4 1 -2
.ENDS
*
*        END OF SUBCIRCUIT
```

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