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High Current Voltage Regulator Module (VRM) Uses DirectFET™ MOSFETs to Achieve Current Densities of 25A/in2 at 1MHz to Power 32-bit Servers

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As presented at Power Systems World, October 2002

***Abstract* - With 1U servers employing dual processor platforms, the current density requirements for voltage regulator modules (VRMs) have increased dramatically. This paper discusses the design of a 1U server type VRM that uses DirectFET packaging technology to enable 120A full load current in a 3.8in x .25in footprint at 82% efficiency. Intelligent integration of the package into the VRM design helped reduce system level parasitics and enabled high efficiency at 1MHz operating frequency.**

INTRODUCTION

In order to make the best possible use of floor space in the server room or data center, users are demanding more and more computing power from 32-bit servers. Consequently, dual processor platforms have now become commonplace even in 1U sized servers. Current requirements for such a system can easily exceed 100A while the 1U size rack severely limits DC-DC converter solution size. To compound the problem, the MOSFETs used in DC-DC converters to power these systems use surface mount package technology (SMT) which to date has offered poor thermal performance with limited heat-sinking options. The main reason for the poor thermal performance of SMT packages such as the SO-8 and its derivatives is that they were designed to be IC packages and even when modified, still offer extremely high thermal and electrical impedance. DirectFET packaging, on the other hand, has been designed from the ground up to be a power semiconductor package and therefore demonstrates how better integration of the package in the DC-DC converter can be achieved when the end application is considered during the early mechanical design. This article discusses how system level parasitics can be reduced by intelligent integration of the new surface mount packaging technology into the VRM design. The result is a VRM capable of a current density of 25A/in^2, enabling a viable solution for next generation processor requirements.

DIRECTFET™ PACKAGING TECHNOLOGY

DirectFET packaging has a unique construction that provides breakthroughs in die free package resistance and heat dissipation capabilities, dramatically increasing efficiency and current carrying capacity of the device in a given footprint.

The DirectFET MOSFET is shown in figure 1. The MOSFET die is a vertical trench power MOSFET. The devices source and gate contacts are formed on the lower surface of the die. The drain electrode on the upper side of the power MOSFET die is connected to a copper 'can' type assembly with conductive adhesive. Drain connections to the device are made via extended pads at the perimeter of the clip. The device can be soldered directly onto a substrate, for example FR4 or polyimide, using conventional surface mount techniques. A proprietary passivation system on the silicon die isolates the gate and the source pads to prevent shorting and acts as a solder mask when the device is mounted on the PCB. The passivation layer also protects the termination and gate structures from moisture and other contamination. This design eliminates the lead-frame and wire bonds, reducing die-free package resistance (DFPR) to a mere 0.1mOhm in an SO-8 footprint compared to 1.5 mOhm for the standard SO-8 package.

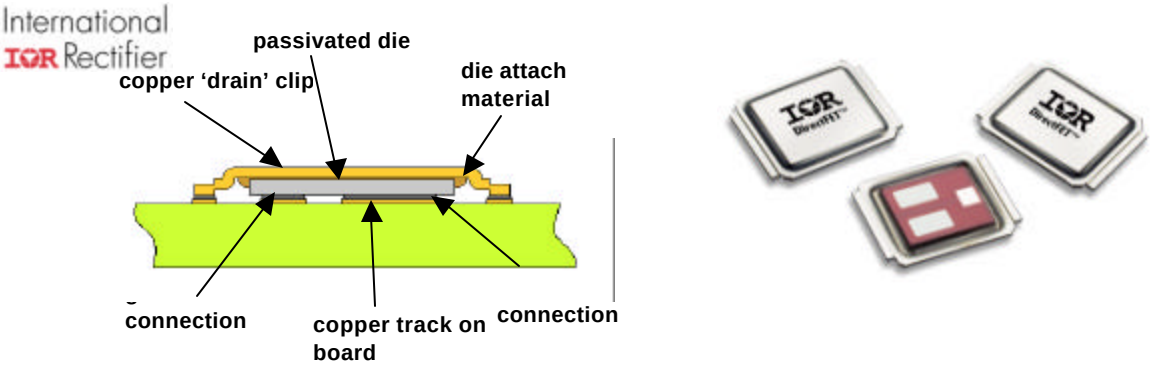

Figure 1. DirectFET Packaging (a) Cross Section (b) Photograph showing bottom side of passivated die

The large-area contacts combined with the copper housing significantly improve heat dissipation compared to a SOIC plastic molded package: the junction-to-PCB thermal resistance is reduced to 1°C/W, compared to 20°C/W for a standard SO-8 package. The copper 'can' provides a heat sink surface, improving top junction-to-case thermal resistance to 3°C/W compared to 18°C/W for a SO-8.

Besides reducing package parasitics, the new packaging technology allows easy layout (see Fig. 2.), simplifying board design and reducing PCB trace losses.

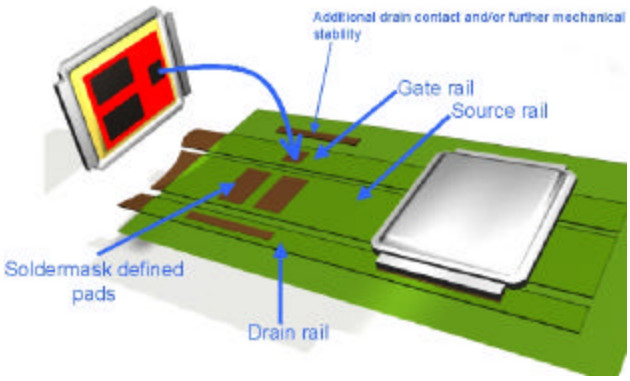

Figure 2. Layout and paralleling of DirectFET devices

VOLTAGE REGULATOR MODULE (VRM) DESIGN

A high current 4-phase VRM was designed using DirectFET MOSFETs as shown in figure 3. The board is 6-layer, 2oz. copper using "pad-in-via" technology. The 4-phase controller and the drivers used in the design are capable of operating at up to 1MHz/phase. The drivers are able to provide drive currents of up to 1.5A and implement an integral diode for the boost drive. To enable a small solution footprint, ceramic capacitors were used for both the input and output filter while the inductor is a 400nH high-current, small footprint coil (10mmX10mm).

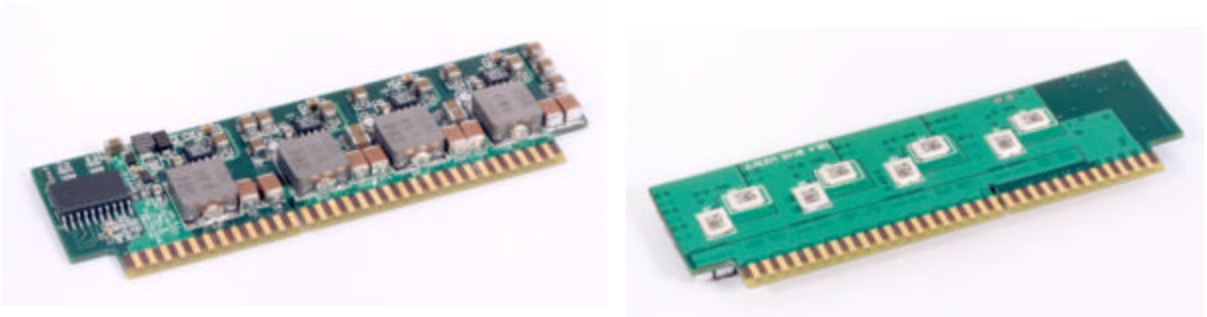

Figure 3. Images of front and rear sides of the 4-phase VRM board with DirectFET MOSFETs shown mounted on the rear side. The heatsink is not shown.

The design is capable of over 100A (> 25A/phase) at high efficiency in a 95mm x 31mm (3.8in x 1.25in) footprint and uses a single control and a single synchronous DirectFET MOSFET per phase. The specifications of the 30V DirectFET control and synchronous FET are shown in Table 1. Note the high current capability (I_D) of both the devices which eliminates the need to parallel devices.

Table 1: Specifications

Part #	$R_{DS(on)}$ mOhm @10V_{GS}	Q_G (nC)	Q_{GD} (nC)	Q_{GS} (nC)	I_D (A)	Function
IRF6603	2.8	69	19	14.5	84*	Synchronous FET
IRF6604	10	20	7	6.8	59*	Control FET

Note: All values typical
* T_{CASE} = 25°C

The low profile of the DirectFET MOSFETs allows the converter design to be configured with the devices on the back of the board and a heat sink to be mounted on top of them while still staying within VRM 9.1 outline specifications. The heat sink is an aluminum finned heat sink measuring in 94mm x 19mm (3.75in x 0.75in x 0.175). It was attached on top of the MOSFETs using an electrically isolating, heat conducting epoxy.

With the use of heatsinks and cooling air flow, the DirectFET package can dissipate more heat out of the top of the package, reducing the operating temperature of the device compared to the SO-8 solution. Effective top-side cooling means that heat dissipated can be pulled away from the circuit board, increasing the currents that the device can safely carry. High top $R_{th(J-C)}$ explains why standard and derivative SO-8 packages are only used with single-side cooling through the PCB. For the purpose of the discussion, consider the model shown in Figure 4 below, which compares the thermal resistances of the standard SO-8 and that of the DirectFET package. For the DirectFET package, the junction to ambient thermal resistance is considerably lower than that of the SO-8 since a heatsink can be used on the top metal can to facilitate removal of heat from the device. Assuming Rth(pcb-a) for the system to be 40°C/W (it could be higher or lower depending on the thermal mass of the PCB) we can see that the DirectFET package allows a much easier path for the heat to be dissipated through the top of the device than the SO-8. This allows more current to be handled by a single device since most of the heat generated is removed and a stable board temperature is maintained.

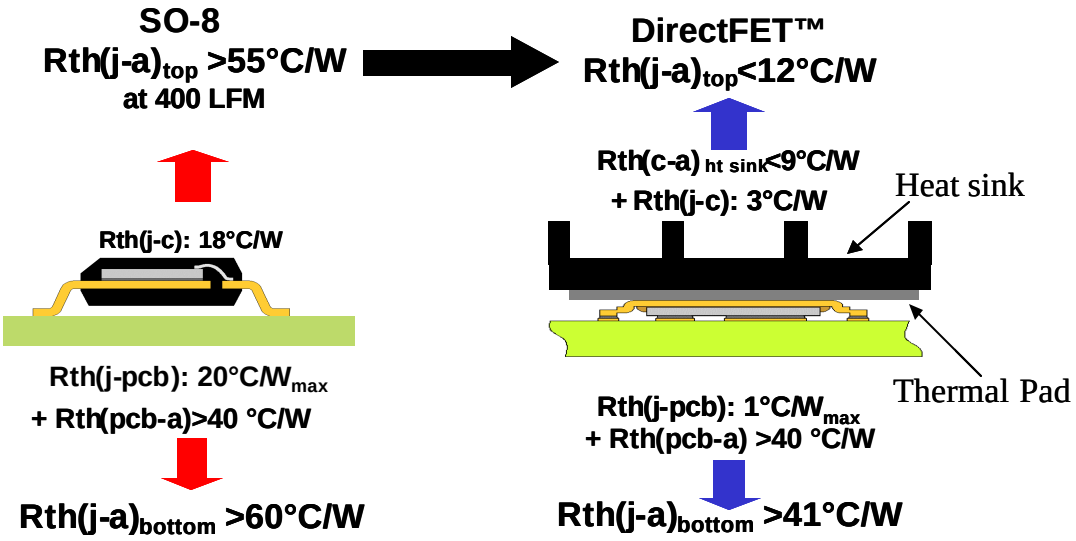

Figure 4. Comparison of thermal model of the DirectFET vs. an SO-8 package

VRM EFFICIENCY AND CURRENT HANDLING CAPABILITY

A VRM with similar current handling capability of 25A/phase SO-8 or D-Pak packaged MOSFETs would require 4-5 devices/phase. In order to dissipate the heat better, the devices have to be laid out in a wider area. The VRM solution footprint for these devices is therefore typically twice that of DirectFET MOSFETs. While the larger solution size is on its own undesirable, the longer traces associated with it also reduce efficiency. In a 4 phase design, the difference in the PCB losses (ΔPD_{PCB}) between the DirectFET design and the SO-8 or D-Pak design is given by:

$$\Delta PD_{PCB} = 4 \times (I_{AV})^2 \rho_{TR}(\Delta L) \qquad \text{-------(1)}$$

Where I_{AV} = Average current/phase = 25A
ρ_{TR} = Trace resistance/unit length for a 0.1inch wide trace on a 2oz. Cu board = 2.5 mOhm/inch
ΔL = Difference in trace length/phase between the SO-8 or D-Pak VRM design versus the DirectFET VRM design = (0.5in)

i.e ΔPD_{PCB} = 3.12W.

The VRM design using DirectFET MOSFETs is therefore, not only smaller, but reduces PCB losses compared to an SO-8 or D-Pak design resulting in a higher efficiency solution.

Efficiency was further optimized using a Schottky diode in parallel with the synchronous FET in the design. Schottky diodes are used in synchronous buck converters to reduce the reverse recovery losses generated in the synchronous FET and dissipated in the control FET. The effectiveness of the Schottky diode is entirely dependent on the loop inductance between the synchronous FET and the Schottky. In most discrete designs, the loop inductance is usually too high for the Schottky diode to improve efficiency, however in the case of the DirectFET design, the low inductance of the DirectFET package allows a ½% efficiency improvement.

Since the MOSFETs have a V_{GS} rating of 20V, they require a gate drive voltage of 5V or above to hard switch the devices. The optimal gate drive voltage for the MOSFETs was found by measuring efficiency at $5V_{GS}$ gate drive and above in of increments of 0.5V. It was found that a gate drive gate drive voltage reached 7.5V and then dropped rapidly after further increments.

The VRM board was redesigned using 4oz. Cu, reducing PCB trace resistance further and improving the thermal performance. Figure 5. shows the efficiency curve generated by this 4oz. Cu VRM operating at 500kHz with an input voltage of 12V and an output voltage of 1.7V with 600LFM airflow. The $7.5V_{GS}$ gate drive offers higher efficiency over a wider range of load current and the VRM delivers a phenomenal 82% efficiency at 120A maximum load current

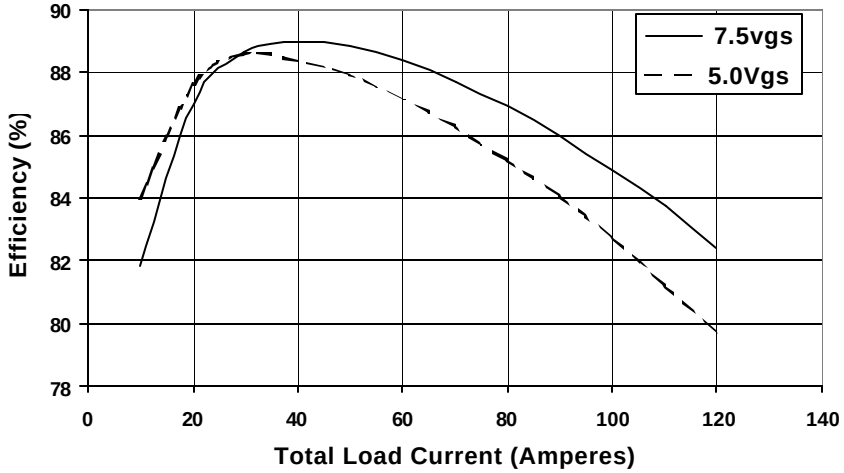

Figure 5. Efficiency at 500 kHz, 12V in, 1.7 V out, in 1U type VRM using DirectFET MOSFETs with 4 oz copper PCB, 4 Phases with 600LFM airflow

At 1MHz the VRM deliver 79% efficiency at 100A full load current as shown in figure 6. The higher operating frequency increases the transient response of the VRM and a fewer number of capacitors would be required near the load to meet the high transient response required when the processor steps from a low-demand processing environment to a high demanding processing environment.

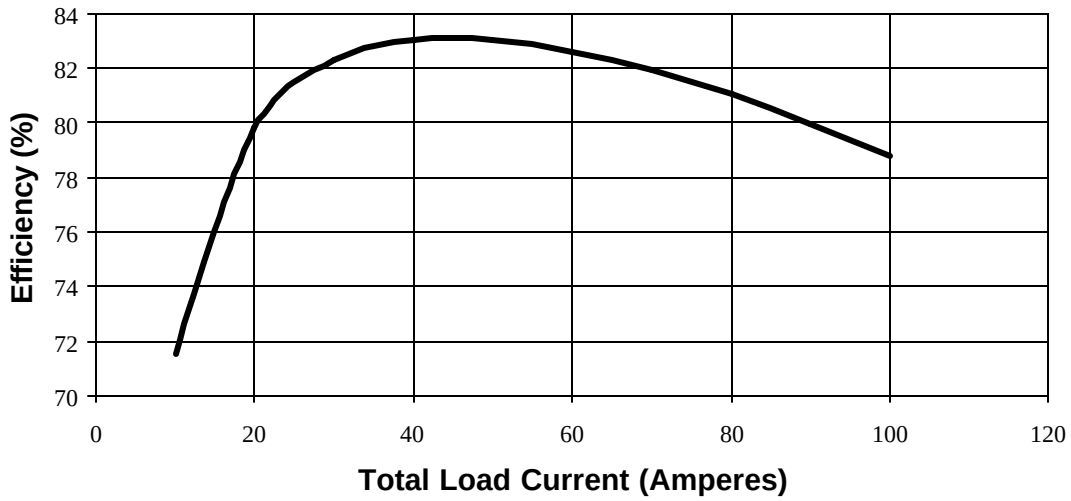

Figure 6. Efficiency measurement at 1MHz on the 4oz Copper board

CONCLUSIONS

This article has demonstrated the design of a 3.8in x 1.25 in VRM, capable of 120A at 82% efficiency when operating at 500kHz. The VRM was found to be able to offer 79% efficiency at operating frequencies of up to 1MHz, reducing ripple while improving transient response. This breakthrough in performance is obtained by combining an innovative packaging technology and intelligent integration into the system design. The implementation of the DirectFET MOSFETs also results in reduced system cost by reducing the number of MOSFETs required, PCB size and and the overall cost of heat removal. Expensive, space consuming thermal management solutions such as heat pipes can also be eliminated. As more and more processing power is crammed into 1U servers driving up current requirements, DirectFET technology could make the task of the VRM designer far simpler.