Design Guidance for the Mechanical Reliability of Low-K Flip Chip BGA Package

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Abstract

Flip Chip Ball Grid Array (FCBGA) package has been introduced in recent years to address the needs in the microelectronic packaging industry for increasing performance and I/O density, which offers a cost effective solution with smaller form factor. Furthermore, Cu interconnects with low-k dielectric material were also introduced to reduce power consumption and further enhance device performance. Due to the nature of low-k dielectric material characteristics, it is more sensitive while a package with low-k material subjected to thermal loading stress.

This work conducted analyses on various FCBGA package design parameters using 3-D finite element method (FEM) and provided design suggestions while selecting the packaging materials. To demonstrate the appropriateness of the finite element models, the modeling results were also calibrated with experimental package warpage measurements. Based on modeling data it was revealed that certain set of packaging materials would further enhance overall package reliability performance. Basic package design guidelines will be presented upon the findings of this study, which products designers could benefit from the superior power consumption and devices performance offered from the integration of Cu interconnect and low-k dielectric.

Keywords: FCBGA, low-k dielectric, finite element method, thermal loading, and thermal stress

Introduction

Flip chip technology has been introduced in recent years to address the demand in the electronic packaging industry for increasing density and performance, as well as lightness, thinness, smallness and cost-effectiveness. By employing the underfill layer, the serious thermal stress that is caused in packages due to thermal expansion mismatches between the silicon die and the organic substrate can be effectively reduced to improve the solder bump reliability [1]. However, some reliability issues have been observed regarding the underfill. The filled underfill causes the package to deform under thermal loading and increases the stress at die-underfill, solder-underfill, and substrate-underfill interfaces, thus can impact the package reliability [2]. Meanwhile, the low-k dielectric has been widely used in the Cu damascene structure of flip chip package and some failures are commonly observed in the low-k layer [3]. Therefore, the low-k reliability becomes an important concern when assembling the die into the flip chip package.

Some researchers [4-8] investigated the low-k interconnection reliability under thermal loading. When the IC device is packaged in the flip chip configuration, the low-k interconnection structure will be subjected to the global bending of the package, because of thermal expansion mismatches between the silicon die and the organic substrate. High thermal stresses are induced at some locations of low-k interfaces. Such thermal stresses may exceed the interfacial strengths, causing the delamination in the low-k interconnection structure, degrading the long term operating reliability of the flip chip package. Consequently, reducing the thermal stress on the low-k interconnection is of primary concern in current flip chip design for enhancing the package mechanical reliability.

To analyze the electronic packages, the 2-D or 3-D finite element method (FEM) is a feasible methodology, which has been widely adopted in the literatures [4-8].

Ho and co-workers [5-7] applied the finite element submodeling technique to evaluate the stress behavior and interfacial cracking of Cu/low-k structures. Mercado et al. [3] also adopted such technique to study the flip-chip die attach process as well as the effects of the residual stresses at both wafer and package levels.

Using a 3-D finite element model, this study investigates the effects of various package design parameters of flip chip ball grid array (FCBGA) package (see Fig. 1) on the low-k reliability under the thermal loading. Various design parameters including die thickness, substrate thickness, underfill material, TIM (Thermal Interface Material) material, adhesive material, and heat spreader type are discussed. Moreover, the appropriateness of finite element models is demonstrated by comparing the predicted die thermal deformation in flip chip package analysis with experimental results measured by shadow moiré.

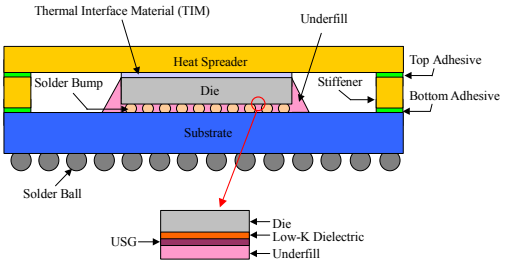


Figure 1. Schematic of FCBGA package configuration.

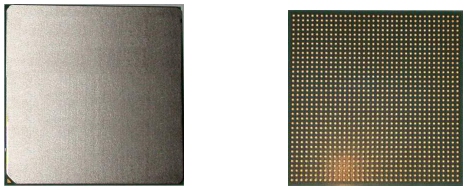
Finite Element Modeling

A 3-D finite element model is constructed using the commercial software, ANSYS®, to perform the package mechanical analysis. The package considered in this present work is a low-k FCBGA with 1296 I/Os in an area-arrayed format, as depicted in Fig. 2. The die size of the FCBGA is 18 × 18 mm with a thickness of 29 mil. The size of the substrate is 37.5 × 37.5 mm, and it has a thickness of 1.1 mm.

Owing to the double symmetry of the FCBGA package, only one quarter of the package was modeled for computational efficiency. Figure 3 displays the 3-D finite element mesh model of the FCBGA package with 30,627 elements and 34,756 nodes. The symmetry boundary condition of the analysis model is defined on the symmetry planes, and the node at the bottom of the intersecting line of these two symmetry planes is constrained to move in the z direction. Table 1 lists the FCBGA package parameter design under consideration, including die thickness, substrate thickness, underfill material, TIM material, and adhesive material. This investigation also explores the effects of three heat spreader types on low-k stress, including two-piece, tunnel, and DLA (Direct Lid Attach) types as shown in Fig. 4.

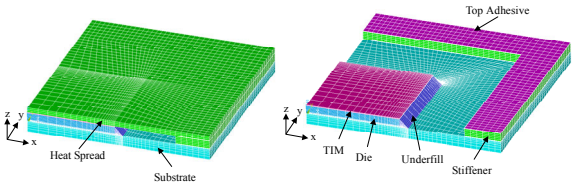
Table 1. Package parameter design for the FCBGA package.

	Die Thickness (mil)	Substrate Thickness (mm)	Underfill Material	TIM Material	Adhesive Material
Baseline	29	1.1	UN-1	TIM-1	AD-1(Top) / AD-1(Bottom)
Parameter Design	19 ~ 29	0.5 ~ 1.3	UN-1 UN-2 UN-3	TIM-1 TIM-2 TIM-3 TIM-4 TIM-5	AD-1(Top) / AD-1(Bottom) AD-1(Top) / AD-2(Bottom) AD-2(Top) / AD-1(Bottom) AD-2(Top) / AD-2(Bottom)



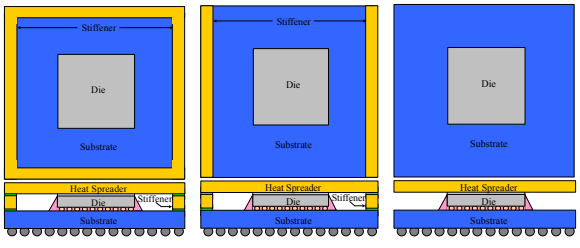
(a) **(b)**

Figure 2. (a) Top view and (b) bottom view of the FCBGA package.



(a) **(b)**

Figure 3. Quarter of 3-D finite element mesh model of the FCBGA package: (a) full model and (b) full model with only heat spreader removed.



(a) **(b)** **(c)**

Figure 4. Various heat spreader design configurations: (a) two-piece, (b) tunnel and (c) DLA types.

Table 2. Material properties of the FCBGA models.

Material	Underfill			TIM					Adhesive		Bump / Eutectic	USG	Low-k	Die	Substrate	Epoxy
Model	UN-1	UN-2	UN-3	TIM-1	TIM-2	TIM-3	TIM-4	TIM-5	AD-1	AD-2						
CTE(ppm/°C) (Below Tg)	32	45	35	58	150	280	232	108	39	46	24.7	1.73	25	2.6	15	69
CTE(ppm/°C) (Above Tg)	110	143	115	220					162	140						
Young's Modulus(GPa) (Below Tg)	7	5.6	7	Stepwise from 6.25@-65°C to 0.019@150°C	0.053	6.0E-05	0.35	0.01	Stepwise from 9.38@-65°C to 0.075@ 150°C	Stepwise from 12@-65°C to 0.1@150°C	30	49.6	13	131	15	3.45
Young's Modulus(GPa) (Above Tg)	0.04		0.04													
Poisson's ratio	0.33	0.33	0.33	0.3	0.3	0.3	0.38	0.3	0.3	0.3	0.4	0.3	0.3	0.28	0.2	0.37

Table 2 shows the material properties of the components of the FCBGA package considered in the finite element analysis. The package in the finite element analysis is subjected to a temperature loading: 125°C to -55°C. The stress-free temperature is assumed to be 125°C. All of the materials in the package assembly are assumed to be linearly elastic, and properties of underfill, TIM, and adhesive in the model are considered to be temperature dependent for both Young's modulus and coefficient of thermal expansion (CTE). In the current analysis, model uses the underfill with effective properties to combine bump and underfill materials.

Shadow Moiré and FEM Validation

To verify the appropriateness of the developed 3-D finite element model, the phase-shifting shadow moiré was employed in this study. Phase-shifting shadow moiré is a photomechanics methodology that can measure the real-time, whole-field, and out-of-plane displacement of the specimen due to temperature variation. The optical arrangement of shadow moiré is illustrated in Fig. 5. In Fig. 5, the white light was adopted as the light source, and the specimen and grating are both placed inside the precision temperature control oven to ensure the uniformity of temperature inside the oven. When the CCD camera was placed as the angle of 45^0 with respect to the incident angle of light, the moiré fringe patterns, which represent the contour of out-of-plane displacement, can be observed. The relationship between the out-of-plane displacement (W) and fringe order (N) is

$$W = N \times P \tag{1}$$

where P is the pitch of grating and it is 50 (lines/mm) in this study. To increase the resolution of shadow moiré, the three steps phase-shifting technique was employed. The distribution of phase can be calculated and it is

$$\theta = \tan^{-1}\left(\frac{I_3 - I_1}{I_0 - I_2}\right) \tag{2}$$

where $I_i\,(i = 0 - 3)$ are the intensities of fringe patterns before and after phase shift was introduced.

Figure 6 shows a package specimen placed in shadow moiré system to verify the appropriateness of the 3-D finite element model. The packaging configuration is the low-k FCBGA (see Fig. 2) with the heat spreader, TIM, stiffener, and top/bottom adhesives removed. Figure 7 shows the 3-D finite element mesh model of the package specimen related to Fig. 6. Considering that the substrate could not endure high temperature, the temperature range in the oven was varied from 120°C to 25°C. Figure 8(a) shows the moiré fringe pattern of the die. Since the solder bump arrangement and the packaging configuration are symmetric, the fringes from the die are like concentric circles. To compare with the moiré experimental

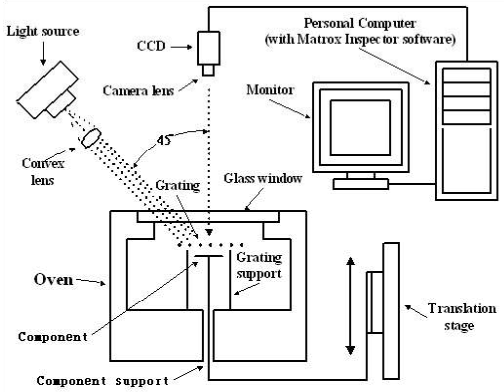


Figure 5. Optical schematic of shadow moiré.

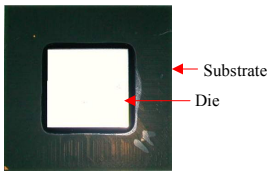


Figure 6. Top view of the package specimen.

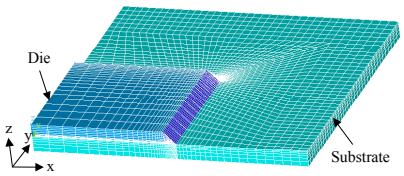
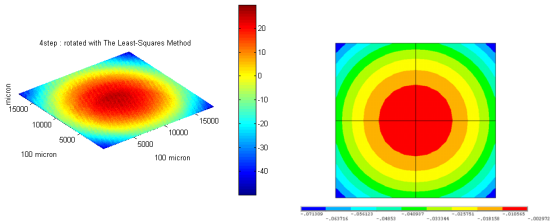


Figure 7. Quarter of 3-D finite element mesh model of the package specimen.



(a) **(b)**

Figure 8. (a) Moiré fringe pattern and (b) simulated thermal deformation contour of the die.

Table 3. Comparison of out-of-plane displacement of the die.

	FEM Analysis	Moiré Experiment
Out-of-Plane Displacement (μm)	70	66

results, the above experimental thermal loading (120°C to 25°C) was applied to the present finite element analysis. The analysis result in the thermal deformation contour of the die is shown in Fig. 8(b). Comparing Fig. 8(a) with Fig. 8(b), the trend in thermal deformation contours of the die obtained from the moiré experiment and FEM simulation are quite similar and the maximum deformation occurs at the corner of the die for the two cases. The analytical and experimental results for the out-of-plane displacement from die center to die corner are listed in table 3 for the package subjected to a temperature testing: 120°C to 25°C. Table 3 shows modeling result is in good agreement with experimental measurement. Consequently, the finite element analysis used in this study is reliable.

Results and Discussion

This work examines the effects of various package design parameters of FCBGA package on the low-k reliability. Design parameters, including die thickness, substrate thickness, underfill material, TIM material, adhesive material, and heat spreader type, are all considered in the 3-D finite element model for estimating the parametric design of low-k reliability. The results of parametric reliability design for the low-k dielectric are shown below. It should be noted that all other parameters are kept constant while the considered parameter is varied.

A. Effect of Die Thickness

To study the effects of die thickness on the low-k reliability, the die with four thicknesses (19mil, 22mil, 25mil, and 29mil) were applied. Figure 9 displays the first principal stress distribution of the low-k dielectric at -55°C for the FCBGA with a die thickness of 29mil. From Fig. 9, maximum first principal stress is induced at the corner area of the low-k dielectric.

Figure 10 presents the maximum first principal stress on the low-k dielectric at -55°C for the package with the die thickness ranges of 19mil to 29mil. From Fig. 10, decreasing the die thickness, the first principal stress will be reduced. This phenomenon occurs because decreasing the die thickness not only reduces the thermal expansion difference between the die and the substrate but also makes the die bend more easily under thermal loading.

B. Effect of Substrate Thickness

This study uses substrates with five different thicknesses, 0.5mm, 0.7mm, 0.9mm, 1.1mm, and 1.3 mm to explore the effects of substrate thickness on the low-k reliability. Figure 11 presents the maximum first principal stress on the low-k dielectric at -55°C for the package with the substrate thickness ranges of 0.5mm to 1.3mm. The maximum first principal stress declines with decreasing substrate thickness.

Consequently, using thinner die or substrate can enhance the low-k reliability.

C. Effect of Underfill Material

Table 4 lists the maximum first principal stress on the low-k dielectric at -55°C when using three different underfill materials such as UN-1, UN-2, and UN-3. The results in Table 4 indicate that applying UN-2 to the package induces the highest stress, while UN-3 leading to the lowest. Using UN-2 will increase the low-k stress by around 24%. Consequently, selecting the underfill material appropriately is important for

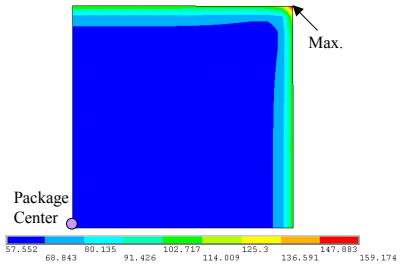


Figure 9. Distribution plot of first principal stress of low-k dielectric at -55°C for the FCBGA package.

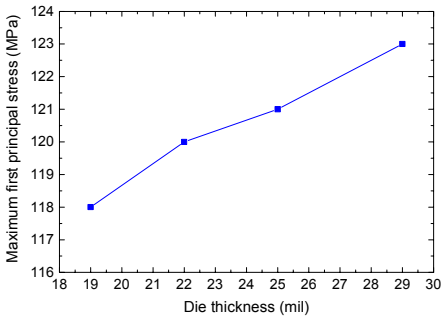


Figure 10. Effects of die thickness on the maximum first principal stress of low-k dielectric.

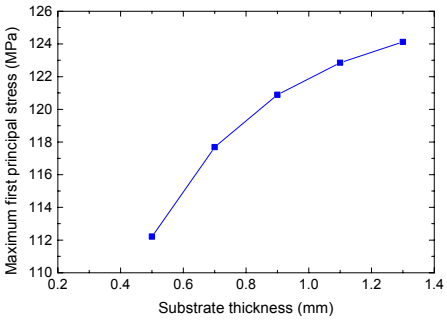


Figure 11. Effects of substrate thickness on the maximum first principal stress of low-k dielectric.

optimizing the low-k reliability and it is recommended that UN-2 should not be applied to the FCBGA package.

D. Effect of TIM Material

Table 5 lists the maximum first principal stress on the low-k dielectric at -55°C when using five different TIM materials, including TIM-1, TIM -2, TIM –3, TIM-4, and TIM-5. The results in Table 5 indicate that applying TIM-1 to the package has the highest stress,

Table 4. Effects of underfill material on the maximum first principal stress of low-k dielectric.

Underfill Material	UN-1	UN-2	UN-3
Max. First Principal Stress (MPa)	123	152	121
Stress Contribution (%)	Baseline	24	-2

Table 5. Effects of TIM material on the maximum first principal stress of low-k dielectric.

TIM Material	TIM-1	TIM-2	TIM-3	TIM-4	TIM-5
Max. First Principal Stress (MPa)	123	88	84	94	86
Stress Contribution (%)	Baseline	-29	-32	-24	-30

Table 6. Effects of heat spreader type on the maximum first principal stress of low-k dielectric.

Heat Spreader Type	Two-Piece	Tunnel	DLA
Max. First Principal Stress (MPa)	123	120	118
Stress Contribution (%)	Baseline	-2	-4

while TIM-3 leading to the lowest. Using TIM-2, TIM-3, TIM-4, or TIM-5 could lower the low-k stress by more than 24%. Consequently, TIM material is a key design parameter for effectively enhancing the mechanical reliability of the low-k dielectric.

E. Effect of Adhesive Material

To study the effects of adhesive material on the low-k reliability, two different adhesive material, AD-1 and AD-2, are applied to four different adhesive configurations, including AD-1(Top) / AD-1(Bottom), AD-1(Top) / AD-2(Bottom), AD-2(Top) / AD-1(Bottom), and AD-2(Top) / AD-2(Bottom). The analytical results show the maximum first principal stress on the low-k dielectric at -55°C is around 123 MPa for all cases. Therefore, this study suggested adhesive material has minimal effect on low-k stress state.

F. Effect of Heat Spreader Type

Table 6 lists the maximum first principal stress on the low-k dielectric at -55°C when using three different heat spreader types such as two-piece, tunnel, and DLA. The results in Table 6 indicate that adopting two-piece design for the package has the highest stress, while DLA design leading to the lowest. Because the

two-piece-type heat spreader restrains the whole package more than the DLA-type heat spreader does and a more internally constrained package would induce larger stresses on the low-k dielectric, DLA design offers the better stress result.

Conclusions

This study examines the effects of various package design parameters of FCBGA on the low-k reliability under thermal loading. 3-D finite element models are used to simulate the thermal-mechanical behaviors of the low-k dielectric. The following conclusions are made based on the analytical results. Firstly, the maximum first principal stress of the low-k dielectric is located at the corner area. Additionally, decreasing the thickness of the die or substrate can reduce the low-k stress. Finally, the key design parameters for effectively enhancing the low-k reliability are packaging materials including underfill and TIM materials. The findings of this study can offer designers and manufacturers an index to adjust the FCBGA design to obtain acceptable low-k reliability.

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