Receiver Offset Cancellation in 90-nm PLD Integrated SERDES

Simar Maangat, Toan Nguyen, Wilson Wong, Sergey Shumarayev, Tina Tran, Tim Hoang, Richard Cliff
Altera Corporation,
101 Innovation Drive
San Jose, CA 95134 USA

***Abstract*– A wide-range transceiver was designed and fabricated in a 90-nm TSMC CMOS logic process. Each transceiver channel contains a transmitter and receiver with Clock Data Recovery (CDR) circuit. The range of operation for this transceiver is from 622 Mbps to 6.5 Gbps. Voltage offsets in the receive path degrade the performance of the transceiver by putting a lower bound on the precision with which a data bit can be measured. In addition to raising the minimum input voltage that can be correctly detected by the CDR, offsets in receive path cause duty cycle distortion, which, added with inter symbol interference (ISI), reduce the overall margin of data recovery directly worsening the bit error rate (BER). Presented in this paper is a methodology to cancel voltage offsets in the receive path with a soft intellectual property (IP) core programmed in the PLD.**

I. INTRODUCTION

The transceiver was designed for a wide range of wireline applications. It supports a variety of protocols including GbE, XAUI, and CEI, which have a lowest input voltage specification. For instance, PCIe-Gen2 places the lower bound for V_{ID} (peak-to-peak input voltage) to be 100 mV. The 3-sigma voltage offset, due to a mismatch in the receiver, was calculated to be a 36-mV differential. This offset eats into the V_{ID} requirement and puts pressure on the CDR, as shown in Fig. 1. The IP developed to cancel the voltage offset in the receive path is implemented in the PLD. It makes use of the data captured by the phase detector (PD) in the CDR and controls the analog hooks in the receiver path to minimize the offset.

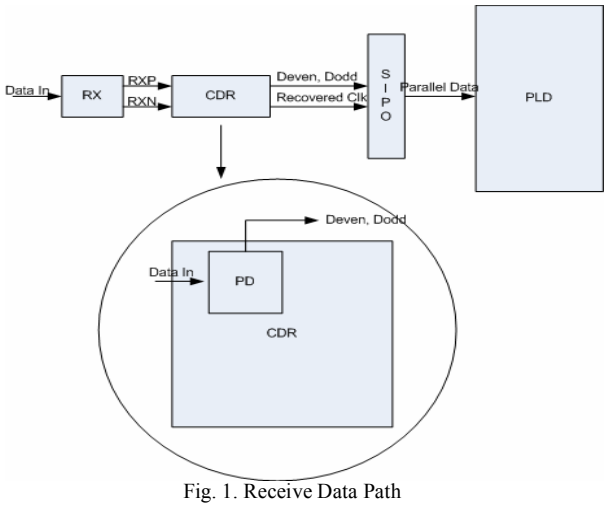


Fig. 1. Receive Data Path

II. RECEIVE DATA PATH OVERVIEW

The Receive Data Path is shown in Fig. 1. The Receiver (RX), which has a 0-dB DC gain, receives the data and relays it to the CDR. The recovered clock and data are then sent to the deserializer or serial-in-parallel-out (SIPO) from where the parallel low-speed data is then sent to the PLD core.

The phase detector (PD) in the CDR is a bang bang phase detector (BBPD). The BBPD is a half-rate non-linear circuit. Half rate refers to the fact that the clock runs at half the rate of the data and that it is non-linear. This is because the output is not a scaler of the phase difference between clock and data. As shown in Fig. 2, the first stage of flip-flops in BBPD is clocked by a 4-phase clock with phases 0, 90,180, and 270 running at half the data rate. The even and odd data are clocked by phases 0 and 180, respectively, and sent to the PLD.

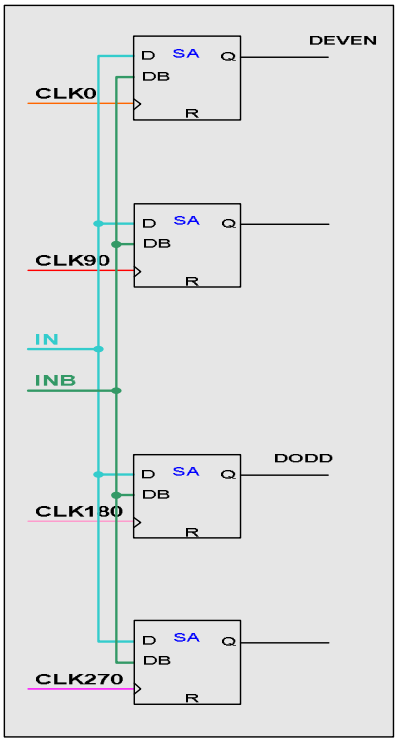


Fig. 2. First Stage of Phase Detector

The BBPD timing diagram is shown in Fig. 3. Phase matching decisions are made by looking at a combinational logic of samples at 0, 90, 180, and 180, 270, 0 respectively. Note that even data corresponds to bit location sampled by phase 0 and odd data by phase 180.

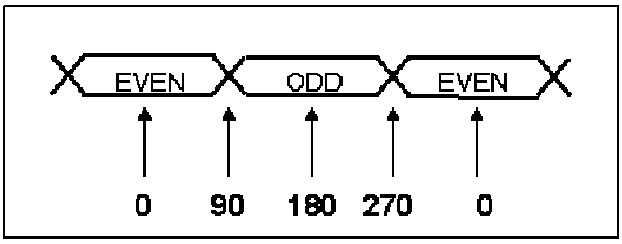


Fig. 3. BBPD Timing Diagram

III. RECEIVE PATH OFFSETS

The offsets in the receive path occur in the RX and the PD. Since the data that is observed is clocked by phases 0 and 180, only those stages of the PD are shown in Fig. 4.

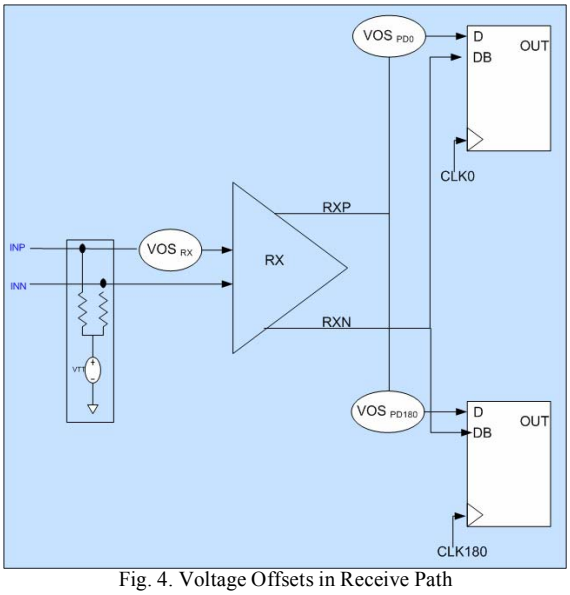


Fig. 4. Voltage Offsets in Receive Path

From Fig. 3, if the offsets of the PD (i.e., VOS_{PD0} and VOS_{PD180}) were zero, then the total offset would just be VOS_{RX}. However, the PD offsets in the worst case scenario be in the opposite direction compounding the total offset.

The voltage offsets caused by a mismatch in the fabrication are getting worse as the technology shrinks. The 65-nm and 45-nm nodes have more of a mismatch problem than the 90-nm node, and increasing the number of legs of devices has a physical limitation. Hence, it is becoming more important to deal with offsets going forward.

IV. OFFSET REDUCTION METHODOLOGY

In the methodology developed, the RX inputs are left floating at the common mode level. Thus, the outputs of the RX, namely RXP and RXN, will exhibit the total RX offset (since the RX gain is 0 dB). Combined with the individual offsets of the PD phases 0 and 180, *Deven* and *Dodd* are sampled and sent to the PLD core. Note that there is no timing issue here for the PD since the data is static and the clock is run at a low frequency of 400 Mhz. A soft controller (IP) programmed in the PLD core analyzes the data and returns digital control to the RX buffer to induce a canceling offset. This is shown in Fig. 5 below.

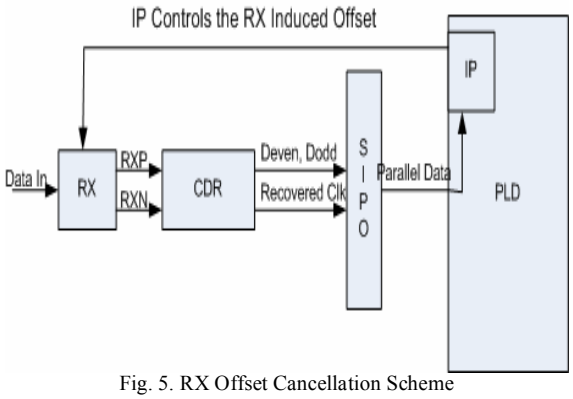
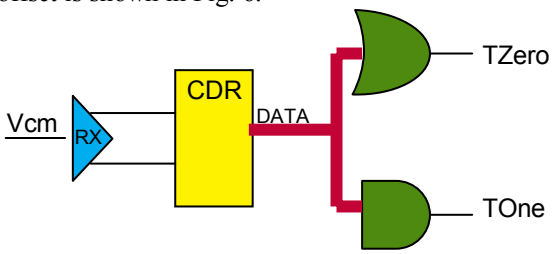


Fig. 5. RX Offset Cancellation Scheme

The induced offset is stepped to both extremes until the data is a stable "1" or a stable "0". The optimum offset cancellation setting is right in the middle of this "unknown" region. A symbolic diagram of the IP that controls the RX-induced offset is shown in Fig. 6.



TZero	TOne	State
0	0	0
1	1	1
1	0	Unknown(X)

Fig. 6. Soft Controller in the PLD

The unknown state happens when the differential voltage RXP-RXN is not large enough to trip the PD phase 0 and 180 both in the same direction. In other words, the 'unknown' region is the aperture of the PD. Therefore, *Deven* and *Dodd* will be of unstable state. The optimum voltage offset setting to result in the lowest V_{ID} is in the center of the 'unknown' region. This concept is illustrated graphically in Fig. 7.

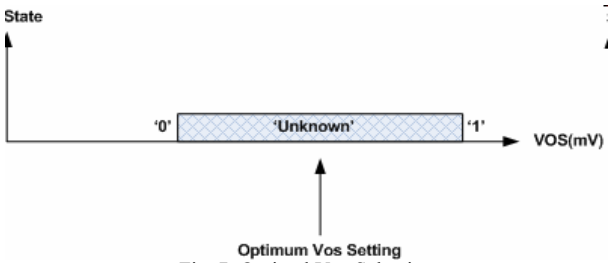


Fig. 7. Optimal Vos Selection

Thus, the offset cancellation scheme averages out the total offset seen at the PD stages 0 and 180 respectively.

V. SILICON RESULTS

The 90-nm silicon measurements were taken with the offset cancellation scheme "on" and "off." The PRBS10 pattern was used for the criteria of BER better than 10e-12 on a sample size of 80 units. The results are promising as the minimum V_{ID} that achieved BER better than 10e-12 has a much tighter distribution. A chart of the measurement data is shown below in Fig. 8:

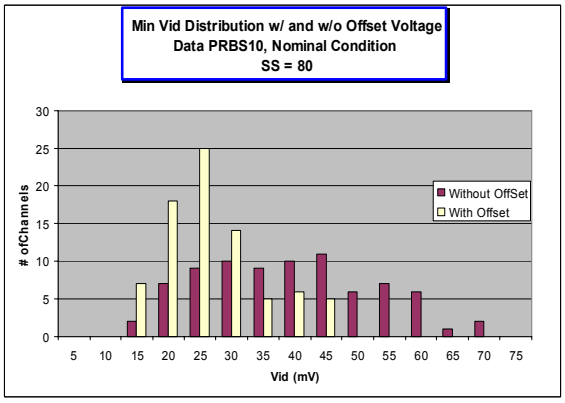


Fig. 8. Minimum V_{ID} w/o Offset Cancellation

Fig. 9 below shows the the minimum V_{ID} required as a function of all the offset settings available. . It is apparent in two of the channels shown below in Fig. 9 that the minimum Vid is achieved by canceling out the offset. For the third channel the random offset is 0, therefore the minimum Vid occurs at the 0 offset setting. This data is taken from within the 80 silicon samples.

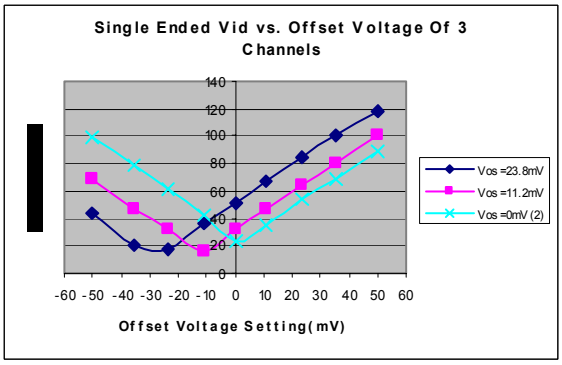


Fig. 9. Minimum V_{ID} vs. Offset Voltage Setting

The last figure, Fig. 10, shows the impact of offset cancellation directly on BER. The measurement data is for a PRBS23 pattern through a 40" FR-4 backplane (which induces large amount of ISI). The chart shows BER vs. offset voltage. Induced offset was stepped through all the settings available and BER was measured. We can see that the relative BER improves by an order of magnitude with offset cancellation "on" for VOS setting of 10 mV or 20 mV.

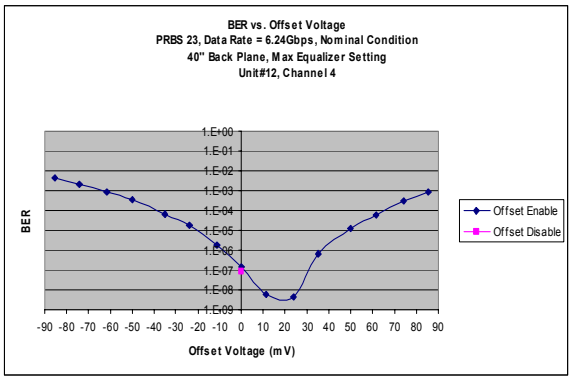


Fig. 10. BER vs. Offset Voltage

VI. CONCLUSIONS

This paper has demonstrated a digitally assisted offset cancellation scheme that was proven on silicon. The offset reduction can improve the performance of a PLD integrated transceiver. The IP-based methodology was found to be an effective replacement for a switch capacitor or feedback amplifier schemes that have certain design impacts and requirements. The results show a tighter V_{ID} distribution directly effecting yield and an improved performance shown by the BER.

ACKNOWLEDGMENTS

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101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
http://www.altera.com