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Setup of a MicroBlaze Processor Design for Off-Chip Trace

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Summary

This application note describes how to modify an existing MicroBlaze™ processor design to support the trace features in MicroBlaze processor v7 and above. It is a detailed tutorial on how to add and configure the trace core in a MicroBlaze processor design. The application note does not target any specific development board, but I/O constraints for some boards are provided to work with Lauterbach and Computex trace tools.

Included Files

Included with this application note are UCF pin constraints for some Xilinx development boards and helper documents for creating UCF pin constraints for other boards. They are available for downloading at:

www.xilinx.com/support/documentation/application_notes/xapp1029.zip

- UCFConstraints.zip - UCF pin constraints for Xilinx boards
- XMTC_Mictor_pinout.pdf - XMTC Mictor pin mappings
- Xilinx_MLBoards_XGI_Expansion_Connector_Interface.pdf - Pin mappings for MLx boards

Hardware and Software Requirements

The hardware and software requirements for this application note are listed below.

- Xilinx Platform Studio EDK9.2.01
- Xilinx Integrated Software Environment (ISE™) 9.2.03i ISE
- Xilinx Platform USB or Parallel IV programming cables for FPGA configuration
- One of the following MicroBlaze trace tools:

  a. Lauterbach PowerTrace and Trace32 IDE

  b. Computex F-Sight MicroBlaze and CSIDE IDE

Introduction

The Xilinx MicroBlaze Trace Core (XMTC) enables the instruction and data tracing of the MicroBlaze processor using an off-chip trace probe from Lauterbach and Computex. It includes a trace encoder, which contains an input interface that attaches to a MicroBlaze processor Trace port composed of approximately 200 un-encoded signals and an output interface that provides an encoded trace in 21 signals. It also includes trigger logic to provide a configurable number of comparators to set trigger conditions based on MicroBlaze processor addresses, data access addresses and values, and register values. The trigger logic can be controlled through the FPGA JTAG interface.

Trace probes and software tools from Lauterbach and Computex are required to capture the MicroBlaze processor trace data and use the data for debugging, program profiling, and code coverage. See the Lauterbach and Computex page for the tool features.

This application note provides steps on how to add the XMTC to the MicroBlaze processor design using Xilinx Platform Studio (XPS). This application note assumes the existence of a MicroBlaze processor v7 design which has been created using Base System Builder (BSB) or XPS. For simplicity it also assumes that there is only one MicroBlaze processor in the design.

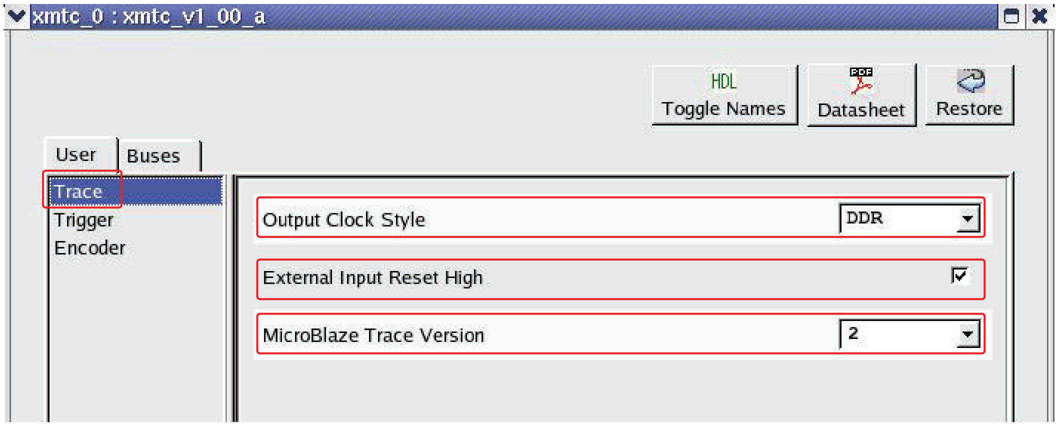
Adding XMTC to the Design

To add the XMTC to the MicroBlaze processor design, the user must:

1. Add and configure the trace core to the MicroBlaze processor design
2. Connect the trace core
3. Add the FPGA pin constraints for the output trace signals

Step 1: Add and Configure the Trace Core to the MicroBlaze Processor Design

1. Instantiate XMTC v1.00a.
   Add `Xilinx MicroBlaze Trace Core (XMTC)` from **IP Catalog** → **Debug** to the System Assembly View.
2. Right click on the **XMTC** instance, select **Configure IP**, then make the selections shown in Figure 1.
   a. Set the Output Clock Style to either **SDR** or **DDR** as required by the trace probe. For Lauterbach PowerTrace, select **DDR** and for the Computex F-Sight, select **SDR**.
   b. Confirm that the External Input Reset High setting.
   c. Set MicroBlaze Trace Version to **2**, which is the trace version available in the MicroBlaze processor v7.



Output Clock Style: DDR

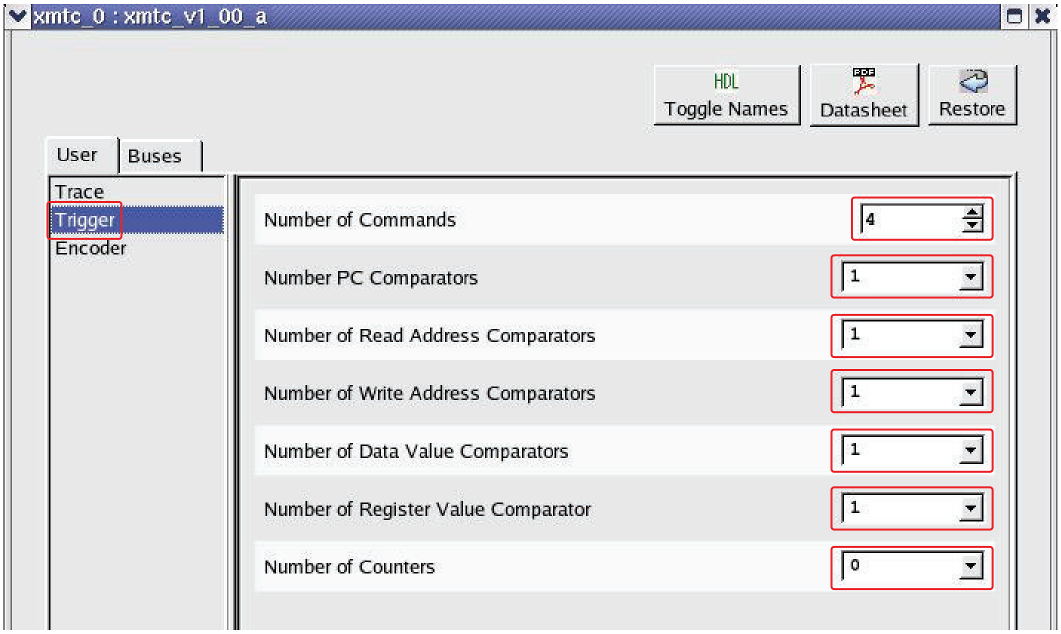
External Input Reset High ☑

MicroBlaze Trace Version: 2

Figure 1: **XMTC Configuration – Trace Interface**

d. Click on **Trigger**, then make the selections shown in Figure 2 to configure the number of comparators required for the particular triggering conditions requirements.

e. Click **OK** to close the **Configure IP** dialog.



Number of Commands	4
Number PC Comparators	1
Number of Read Address Comparators	1
Number of Write Address Comparators	1
Number of Data Value Comparators	1
Number of Register Value Comparator	1
Number of Counters	0

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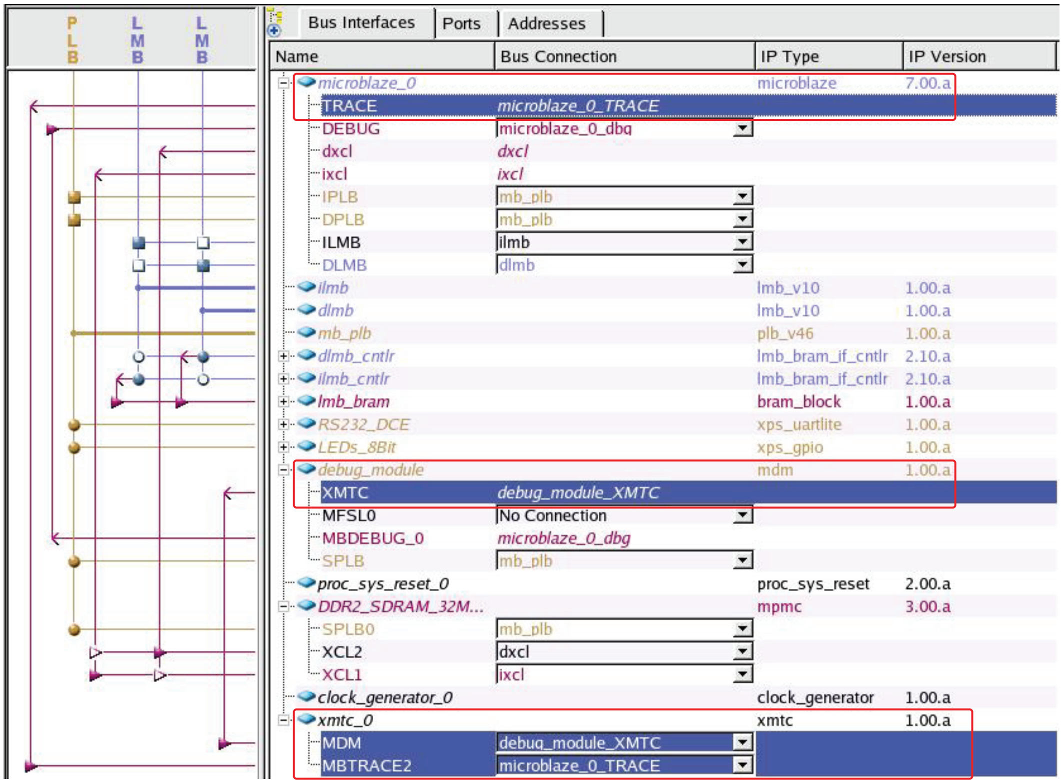
Figure 2: **XMTC Configuration – Trigger Configuration**

Step 2 - Connect the Trace Core

In the Bus Connections window, make the selections shown in Figure 3.

1. Connect the MDM bus interface in XMTC to the XMTC bus interface in MDM.
2. Connect the MBTRACE2 bus interface in the XMTC to the TRACE interface in the MicroBlaze processor v7.00.a.



Name	Bus Connection	IP Type	IP Version
microblaze_0		microblaze	7.00.a
TRACE	microblaze_0_TRACE		
DEBUG	microblaze_0_dbg		
dxcl	dxcl		
ixcl	ixcl		
IPLB	mb_plb		
DPLB	mb_plb		
ILMB	ilmb		
DLMB	dlmb		
ilmb		lmb_v10	1.00.a
dlmb		lmb_v10	1.00.a
mb_plb		plb_v46	1.00.a
dlmb_cntlr		lmb_bram_if_cntlr	2.10.a
ilmb_cntlr		lmb_bram_if_cntlr	2.10.a
lmb_bram		bram_block	1.00.a
RS232_DCE		xps_uartlite	1.00.a
LEDs_8Bit		xps_gpio	1.00.a
debug_module		mdm	1.00.a
XMTC	debug_module_XMTC		
MFSL0	No Connection		
MBDEBUG_0	microblaze_0_dbg		
SPLB	mb_plb		
proc_sys_reset_0		proc_sys_reset	2.00.a
DDR2_SDRAM_32M...		mpmc	3.00.a
SPLB0	mb_plb		
XCL2	dxcl		
XCL1	ixcl		
clock_generator_0		clock_generator	1.00.a
xmtc_0		xmtc	1.00.a
MDM	debug_module_XMTC		
MBTRACE2	microblaze_0_TRACE		

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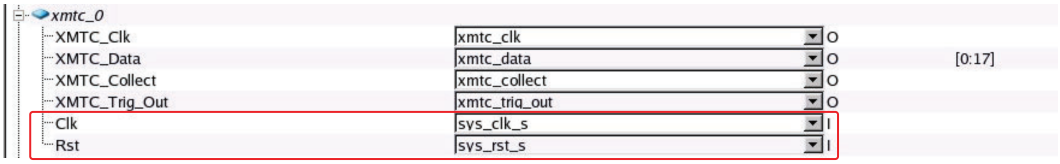
Figure 3: **XMTC Core Bus Connections**

3. Switch to the **Ports** view.
4. Connect the *Rst* and *Clk* ports to the system reset and clock signals respectively. Assign names to the *XMTC_** ports as shown in Figure 4.

Note: If the XMTC_* ports are not visible, select the **Defaults** in the Filter Ports for the XMTC core.



xmtc_0			
XMTC_Clk	xmtc_clk	O	
XMTC_Data	xmtc_data	O	[0:17]
XMTC_Collect	xmtc_collect	O	
XMTC_Trig_Out	xmtc_trig_out	O	
Clk	sys_clk_s	I	
Rst	sys_rst_s	I	

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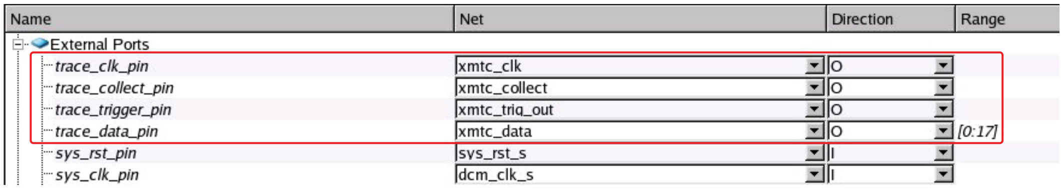
Figure 4: **XMTC Ports View**

5. Under External Ports, create the four trace ports and connect to the XMTC ports as shown in Figure 5. This brings the encoded trace signals to the FPGA I/O pins, which can be monitored by the trace tool.



Name	Net	Direction	Range
External Ports			
trace_clk_pin	xmtc_clk	O	
trace_collect_pin	xmtc_collect	O	
trace_trigger_pin	xmtc_trig_out	O	
trace_data_pin	xmtc_data	O	*[0:17]*
sys_rst_pin	sys_rst_s	I	
sys_clk_pin	dcm_clk_s	I	

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Figure 5: **XMTC External Ports View**

Step 3: Adding FPGA pin constraints for the output trace signals

The Lauterbach and Computex trace cables require the encoder output trace signals to be on different FPGA pins. The zip file (www.xilinx.com/support/documentation/application_notes/xapp1029.zip) provides the UCF pin constraints for different Xilinx boards. Select the UCF constraint file for the partner tool and board, and add these constraints to the `<EDK Project>/data/system.ucf` file.

If the UCF pin constraints for the board being used are not included in this application note, refer to the additional documents in the zip file to create a UCF pin constraints or contact Lauterbach or Computex for FPGA pin constraints.

After completing these steps the user will be able to attach the debugger to the Mictor connector of the board or use one of the adapter provided by third party vendors. Contact Lauterbach or Computex for more details.

References

1. Lauterbach - http://www.lauterbach.com
2. Computex - http://www.computex.com

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
2/7/08	1.0	Initial Xilinx release.

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