Designing a Four-Channel, Return-to-Zero, Ultrasound Pulser Using Supertex HV7370 & HV748 ICs

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Introduction

The Supertex HV7370 is a four-channel, high speed, high voltage, ultrasound transmitter damper, and the HV748 is a four-channel, high speed, high voltage ultrasound transmitter pulser. Both integrated circuits (ICs) are designed for medical ultrasound imaging applications. They can also be used as piezoelectric, capacitive or MEMS sensors in ultrasonic nondestructive detection and sonar ranger applications. These high performance CMOS ICs are in 5x5x0.9mm 32-lead QFN (HV7370) and 7x7x0.9mm 48-lead QFN (HV748) packages.

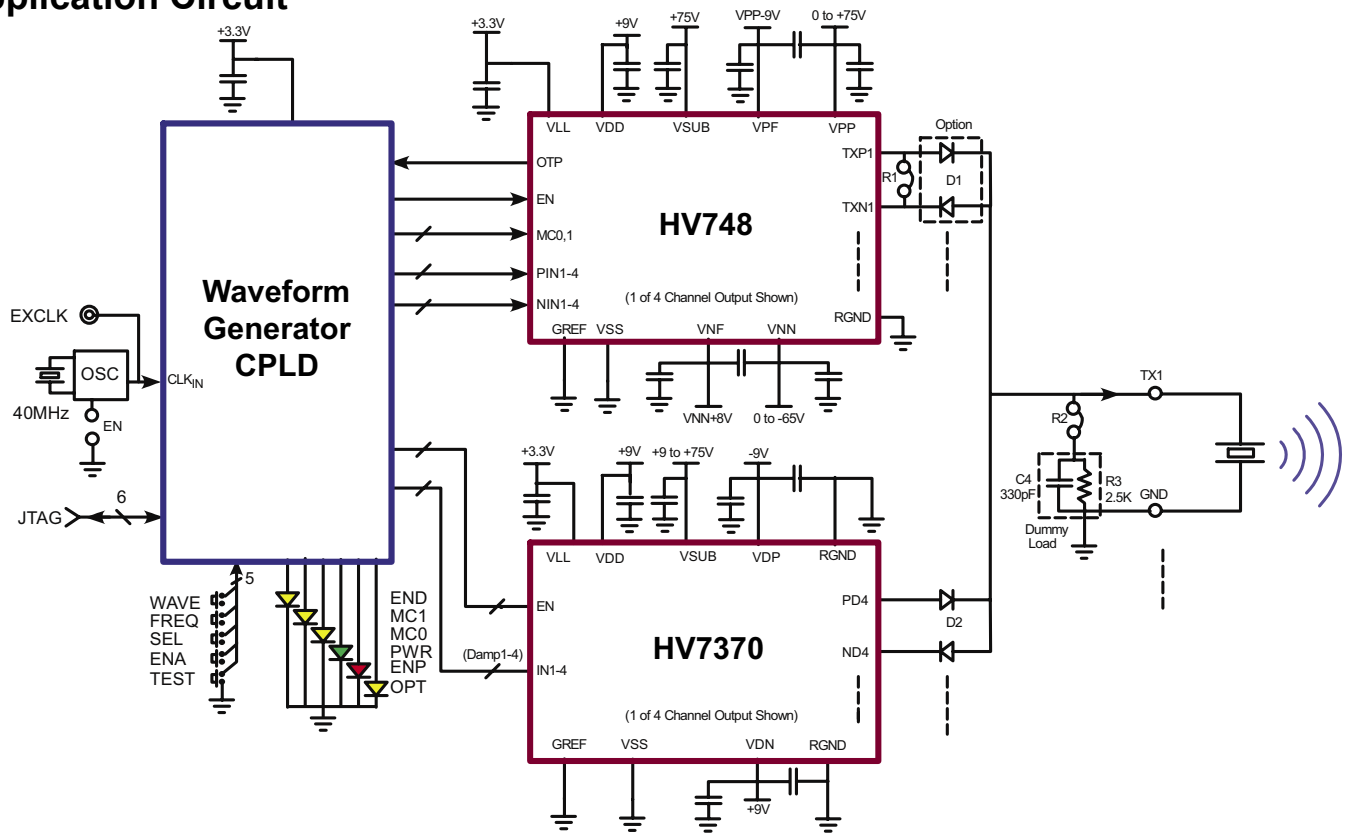
The HV7370 can be also used as a damping circuit with Supertex's HV738 and HV758 pulsers to generate fast return-to-zero waveforms. Depending upon the load capacitance, the frequency limit of this IC is as high as 20MHz.

HV7370 consists of four controller logic interface circuits, four level translators, four MOSFET gate drivers and four pairs of high current N- and P-channel MOSFETs that serve as the four push-pull output stages.

The output stages of each channel are designed to provide peak damping currents over ±0.85A with up to ±100V pulser (V_{PP}/V_{NN}) voltage. The HV7370's N- and P- MOSFET gate drivers are supplied by ±5~12V (typical 8.0 to 11V) on V_{DN} & V_{DP} pins.

The voltages V_{DN} and V_{DP} are referenced to ground (0V). The output pins of the HV7370 (PD1~4 and ND1~4) are able to pull down from or up to ±100V on the capacitive loads, which have been charged by the high voltage pulser channels. However, the V_{PP} and V_{NN} of the HV748 high voltage pulser on this demoboard can only go up to ±75V. The damping action of the HV7370 is independently controlled by the damper input logic signals IN1 to IN4.Internally the logic signal controls a direct-coupled low voltage to high voltage lever translator to switch the output MOSFETs. This direct coupling topology of the gate drivers not only saves two high voltage capacitors per channel, but also makes the PCB layout easier.

Application Circuit



Designing an RTZ Pulser using Supertex's HV7370 & HV748

This application note describes how to use the HV7370 damper and the HV748 pulser to design a high speed return-to-zero (RTZ) pulser.

The output of the damper must go through two DC blocking diodes to connect to the pulser output as the schematic shows. Having the diode pair D1 connected in series with the pulser output is optional because in the three-level RTZ pulser design, the pulser's V_{PP}/V_{NN} supplies are the highest/lowest voltage rails, and therefore there is no need for the DC-blocking function.

The diode pair D2 are necessary, however. Because the damper's MOSFETs have both sources connected to RGND, both damping outputs must have the DC blocking diode in series before they connect to the pulser's output summing node. These diodes are directing current and blocking any reverse current that would otherwise pass through a MOSFET body diode. If one is going to design a five-level RTZ pulser, then the output of the middle level pulser should also have these current steering diodes. Usually these diodes must be high voltage, high peak current and fast reverse recovery time diodes.

The input stages of both HV7370 and HV748 are high-speed level translators that are able to operate with logic signals of 1.8 to 5.0V and are optimized for 2.5 to 3.3V. In most medical imaging systems, these control signals are from an FPGA. If the control line traces are longer than about 2 inches (50mm), it is suggested that each control line should have a 50Ω resistor in series, located near the FPGA output pin, for impedance matching to the 50Ω impedance of their PCB traces.

In this design example, the control logic signal is generated from an on-board CPLD chip. The control logic line is very short; therefore the series resistors are not needed. The logic level of this CPLD is 3.3V on this design example board. The programmable CPLD uses a 40MHz crystal oscillator as the on-board clock to generate a fast clock signal to control the timing of this RTZ pulser.

There are six-pin JTAG connections for the USB or parallel CPLD programming link-cable. Users can easily modify the test waveforms according their own test pattern requirements.

There is also an external clock input in this design example. By inserting a shorting jumper, which disables the on-board oscillator, the user can instead connect an external 3.3V clock.

There are five push buttons for selecting the test waveform, frequency, select, enable and test functions. There are six color LED indicators associated with these push button control functions. There are four on-board equivalent-loads, and each one has a 330pF capacitor in parallel with a 2.5KΩ 1W resistor via the small copper trace shorted zero Ω resistors connected to the RTZ pulser outputs for each channel. The user can easily evaluate the transducer(s) with this HV7370 and HV748 RTZ transmitter pulser. Just open the short(s) and, using the coaxial cable, directly connect to the output test points to the transducer.

PCB Layout Techniques

It is important that the thermal slab at the bottom of the HV748 package be externally connected to its V_{SUB} pins to make sure that it always has the highest potential in any condition, because this is the connection of the IC's substrate.

In order to guarantee that the HV748 V_{SUB} will never be below its other voltage rails, even during the power-up or down time periods, it is strongly recommended that a set of Schottky diodes be added to the PCB of the pulser circuit. Each voltage supply rail must have a 2~3A Schottky diode connected to ground as part of the normal protection scheme used in multi-rail CMOS power supply design. We suggest that you add two more diodes for power up/down protection: one Schottky from V_{CC}, V_{LL} (+3.3V in this design) to V_{DD}, and other one from V_{DD} to V_{SUB} of HV748. Adding these two additional Schottky diodes means that the system can power-up the V_{CC} +3.3V first, then power-up the V_{DD} second, all before turning on the HV748 V_{SUB} voltage. To have the V_{CC} turned on first is very practically important in system power sequence design, because it allows the CPU and FPGA control circuit to be up working first or powered down last, thus allowing all the other voltage rails to be under CPU and logic control. Furthermore, once the CPU and control logic are working, these should immediately initialize all pulser and damper chip enable and control signals to zero. After V_{CC} is powered-up with the said Schottky on board, the V_{DD} and VSUB voltage will be only one or two Schottky diodes' forward-drop voltage away from the V_{CC} voltage. This will protect the IC from having substrate bias voltage reversal or latch up.

The V_{DD} rail (+8 to +12V) provides internal bias and low side control circuits supply voltage in both HV748 and HV7370. In most cases, the V_{DD} or the unregulated V_{DD} voltage source will also be used for the input power supply of the isolated DC/DC converter for the two floating rails (V_{PP} - V_{PF}) and (V_{NF} - V_{NN}), and for the non-isolated DC/DC converter (for -9V V_{DP} etc.). Turning the V_{DD} supply on is second in the power-up sequence and can be under CPU or logic control.

It is also important to make sure that the thermal slab at the bottom of the HV7370 package be externally connected to HV7370's V_{SUB} pin and that the HV7370 V_{SUB} pin be connected to its V_{DD} or HV748's V_{SUB} voltage. It is recommended to have 0.1~0.22µF capacitors decoupling for both HV748 and HV7370 V_{SUB} and placed very close to the pins.

Designers need to pay attention to the connecting traces as high-voltage and high-speed traces. In particular, low capacitance to the ground plane and larger trace spacing is required.

Use high-speed PCB trace design practices that are compatible with about 50 to 100MHz operating speeds. The internal circuitry of the HV7370 and HV748 can operate with high frequencies, with the primary speed limitation being load capacitance. Because of this high speed and the high transient currents that result when driving capacitive loads, the supply voltage bypass capacitors should be as close to the pins as possible. The G_{REF} and V_{LL} are the low and high logic level reference pins that should connect to the control logic circuit ground and V_{CC} voltage, with a 0.1uF ceramic decoupling capacitor connected in between.

The V_{DD}, V_{DN}, V_{DP}, V_{PP}, V_{NN} and V_{SUB} pins are voltage supplies referenced to ground. The MOSFET gate-driver floating supplies (V_{PF} and V_{NF}) are referenced to V_{PP} and V_{NN} high voltage power supplies respectively. All these power supply rails can be shared for multiple HV748 and HV7370 chips if there are a large number of transmit channels in the system. All the power supply pins of each channel can draw fast transient currents of up to ±0.8 to ±1.25A, so they should be provided with a low-impedance bypass capacitor located close to the pins. Use an X7R or X5R 0.47 to 1.0µF ceramic capacitor for each pin or or pair of pins. All by-pass capacitor ground pads should have low inductance feed-through via connections that are connected directly to a solid ground plane. Minimize the trace length to the ground plane, and insert a ferrite bead low value resistor in the power supply lead to the capacitor to prevent resonance in the power supply lines.

Pay particular attention to minimizing trace lengths and using sufficient trace widths to reduce inductance. Surface mount components are highly recommended. Since the output impedance of pulser HV748's and damper HV7370's output stages is very low, in most cases it is desirable to add a 5 to 18Ω pulser current rated resistor in series with the output to obtain better waveform integrity at the load transmission line terminals. This will, of course, reduce the output voltage slew rate at the terminals of a capacitive load.

Be aware of the parasitic coupling from the outputs back to the input signal terminals of the HV7370 and HV748. This feedback may cause oscillations or spurious waveform shapes on the edges of signal transitions. Since the input operates with signals down to 1.8V, even small coupling voltages may cause problems. The use of a solid ground plane and good power and signal layout practices will prevent this.

Testing the Integrated Pulser

This HV7370 and HV748 RTZ pulser design example is tested with multiple lab DC power supplies with current limiting functions. The following power supply voltages and current-limits settings are used in the testing: V_{PP} +75V 2.5mA; V_{NN} -75V 2.5mA; V_{DD} +9.0V 20mA; V_{DN} +9.0V 5mA; V_{DP} -9.0V 5mA; V_{PF} and V_{NF} two isolated DC/DC floating 9.0V 5mA.; and V_{CC} and V_{LL} +3.3V 70 to 80mA. The +3.3V supply current is mainly for the V_{CC} current of the +3.3V-only CPLD.

The on-board dummy load 330pF//2.5kΩ is connected to the RTZ pulser output through the zero Ω resistor on board with default as shorted for using the oscilloscope high impedance probe to look at the output waveforms as the typical load condition. For looking into the different loading conditions, one may change the values of dummy loads within the current and power limitations of the device.

In order to drive the user's piezo transducers with a cable, one should connect each output in series with a small 6.2Ω to 22Ω pulse current rated resistor to match the load and cable impedance properly. This is to avoid large cable and transducer reflections. Usually the ultrasound cable is 50Ω to 75Ω impedance rated.

The on-board test point is designed to work with high impedance probes of the oscilloscope. Some probes may have limited input voltage. When using a probe on the test-points of the pulser outputs, make sure that VPP/VNN does not exceed the probe limits. Using the high impedance oscilloscope probe on the onboard test points, it is important to have as short ground leads to the circuit board ground plane as possible.

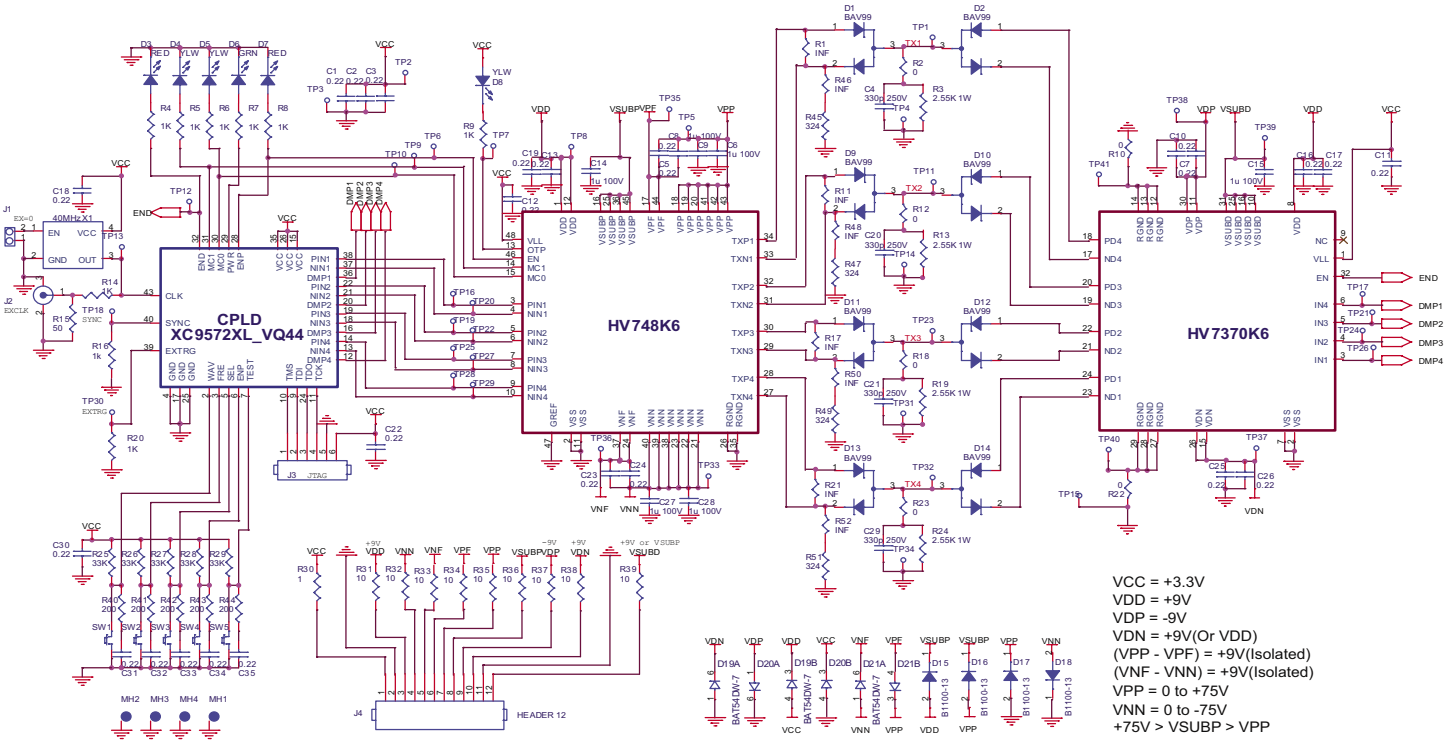
There are multiple frequency and waveform combinations that can be selected as bipolar pulses and PW with and without RTZ waveforms. The frequency of the pulses are 10, 5, 2.5MHz, etc. If one needs a specific transducer frequency, an external clock input can be used instead if the on-board 40MHz-oscillator is disabled with a jumper shorted to ground. There are push buttons for selecting the waveform, frequency, phase, and HV748 & HV7370 chip enable functions. Color LEDs indicate the test selection states.

The HV7370 & HV748 RTZ pulser circuit schematic, input and output waveforms diagrams, detailed signal definitions, and testing of measured waveforms are shown below.

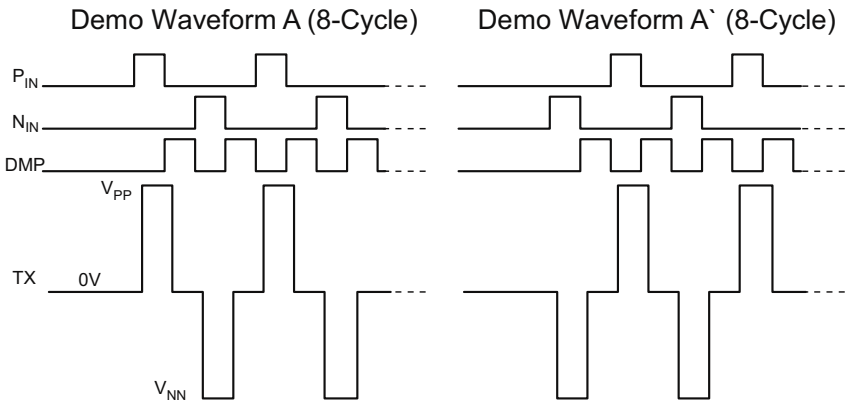
There are push buttons for selecting the waveform, frequency, phase, and HV748 & HV7370 chip enable functions. Color LEDs indicate the demo selection states.

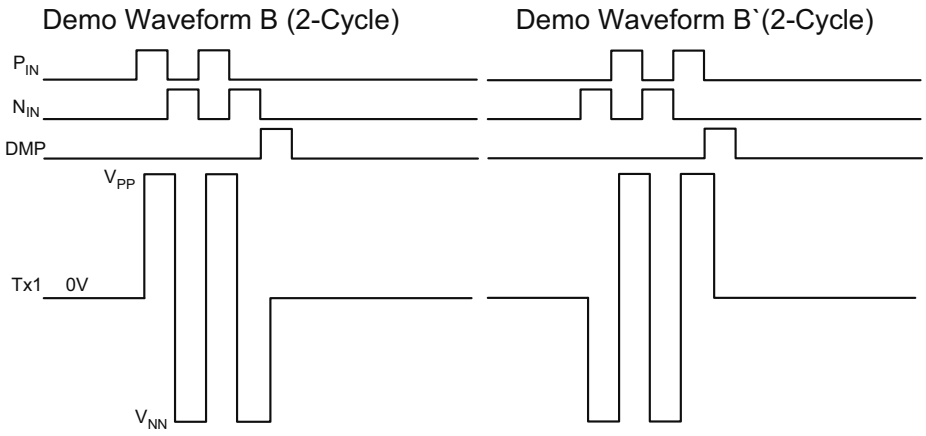
The HV7370DB1 RTZ pulser circuit schematic, input and output waveforms diagrams, detailed signal definitions, and testing of measured waveforms are shown on the following pages.

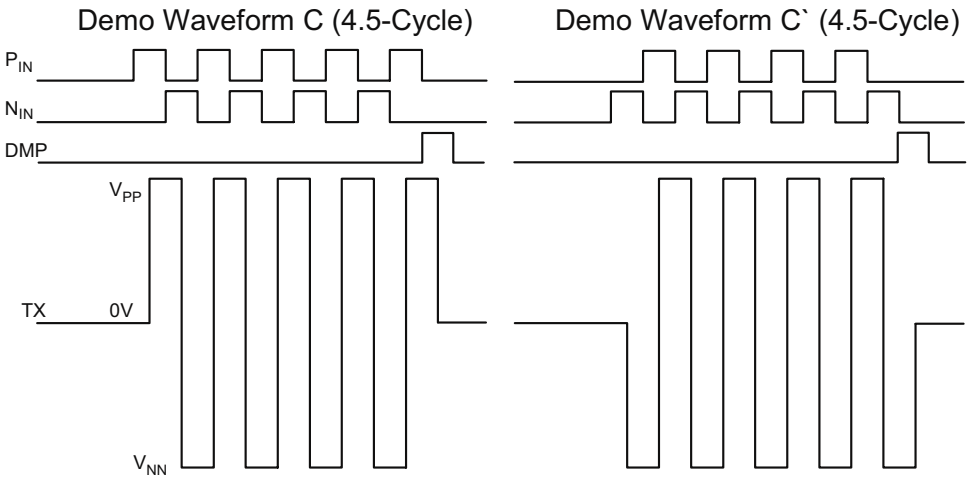
HV7370 RTZ Pulser Schematic



HV7370 RTZ Pulser Waveforms

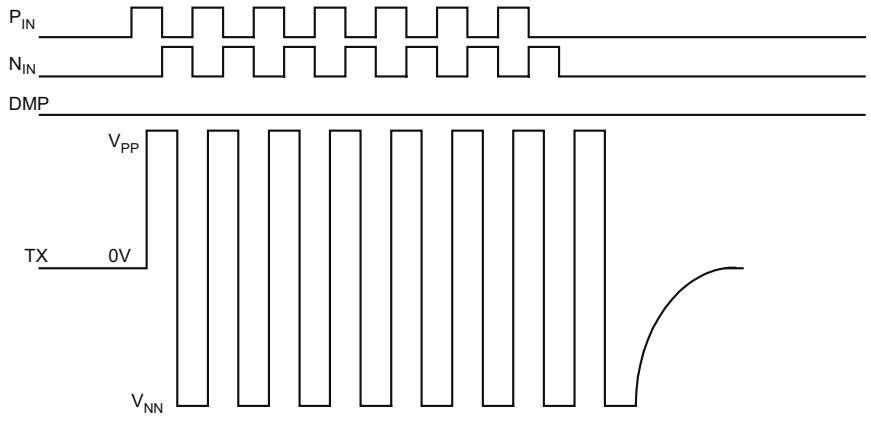




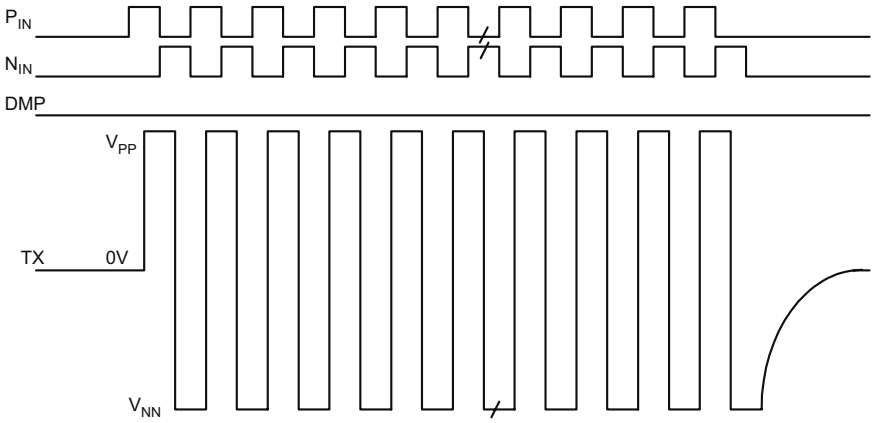


HV7370 RTZ Pulser Waveforms *(cont.)*

Demo Waveform D (8-Cycle w/o Damping)



Demo Waveform E (16-Cycle w/o Damping)

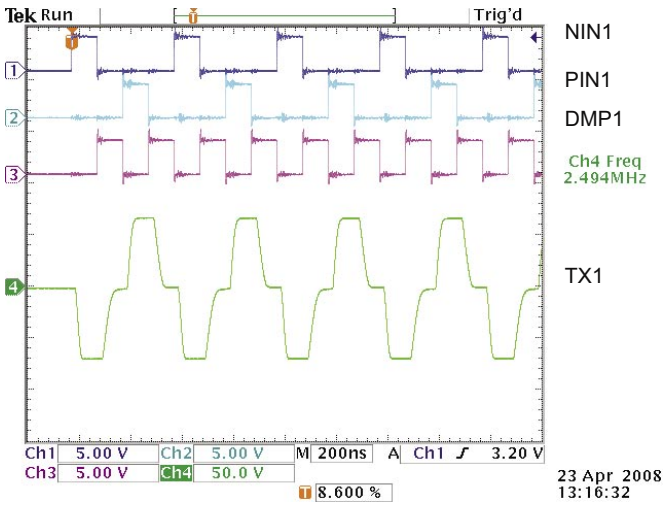


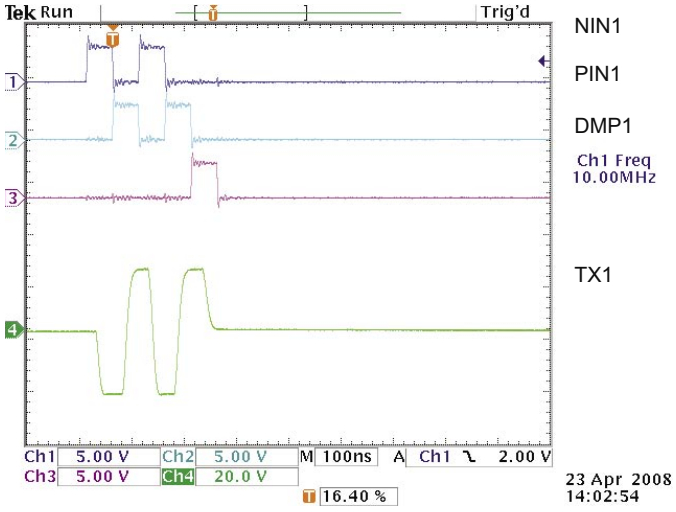
Voltage Supply Power-Up Sequence

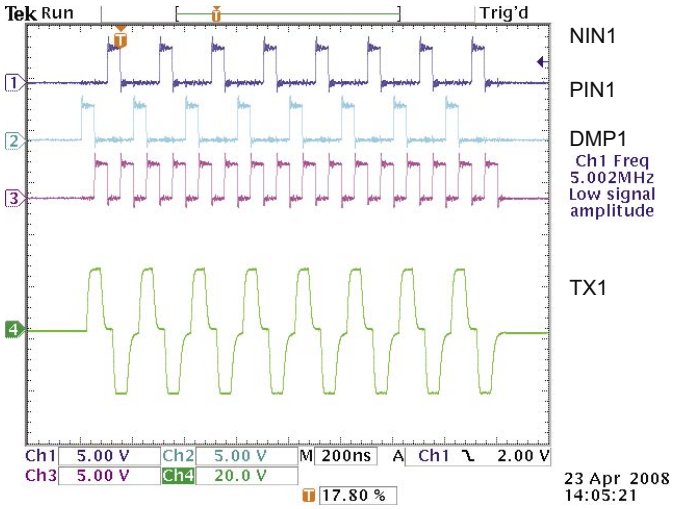
1	VCC & VLL	+3.3V positive logic voltage. (U2 CPLD 3.3V only).
2	VDD, VDN /VDP, (VSUBD)	±9.0V positive drive voltage. (If VSUBD = +9.0V).
3	VSUBP, (VSUBD)	+75V positive high voltages. (VSUBD can be +75V or +9.0V).
4	(VPP- VPF), (VNF- VNN)	Two isolated floating 9.0V.
5	VPP / VNN	±0 to 75V positive and negative high voltages.

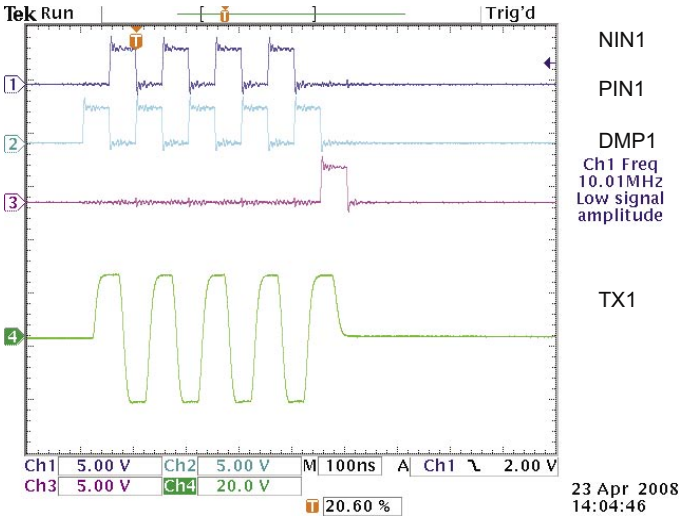
Note:
The power-down sequence is the reverse.

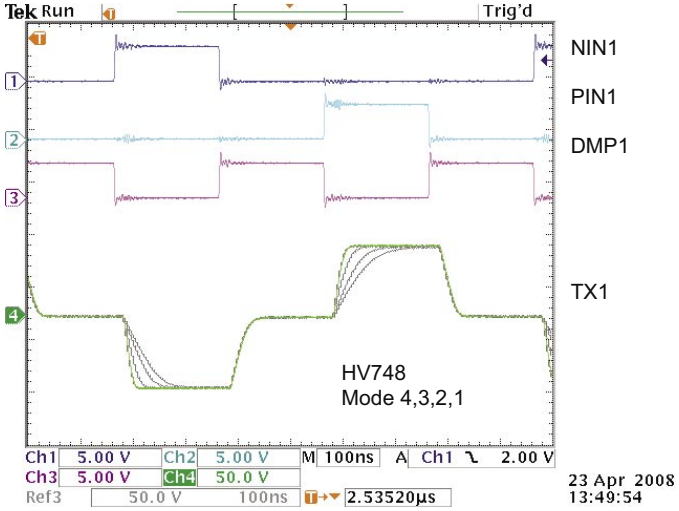
HV7370 RTZ Pulser Waveform Screens

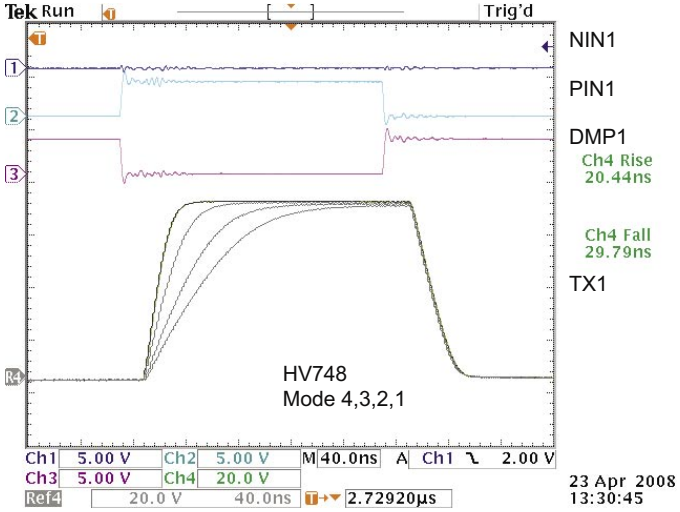




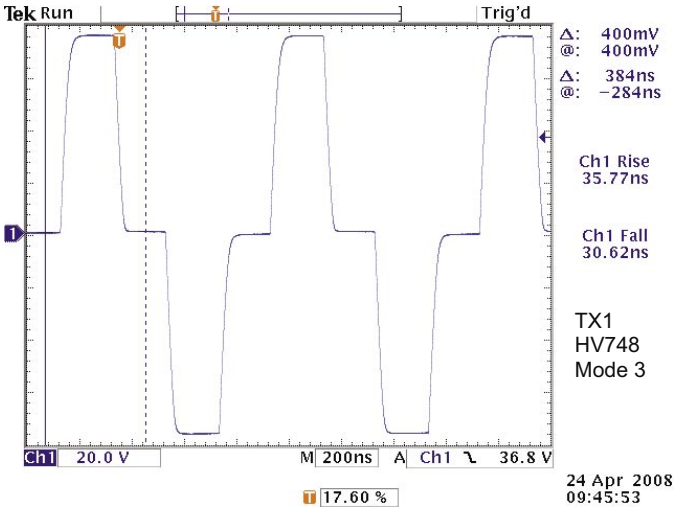


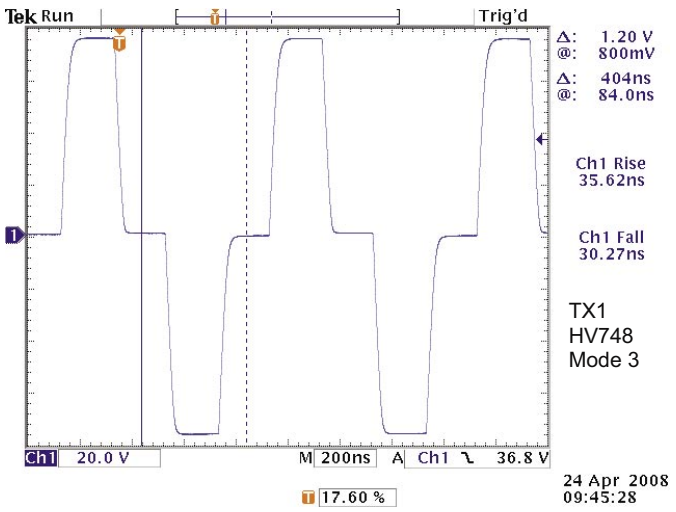


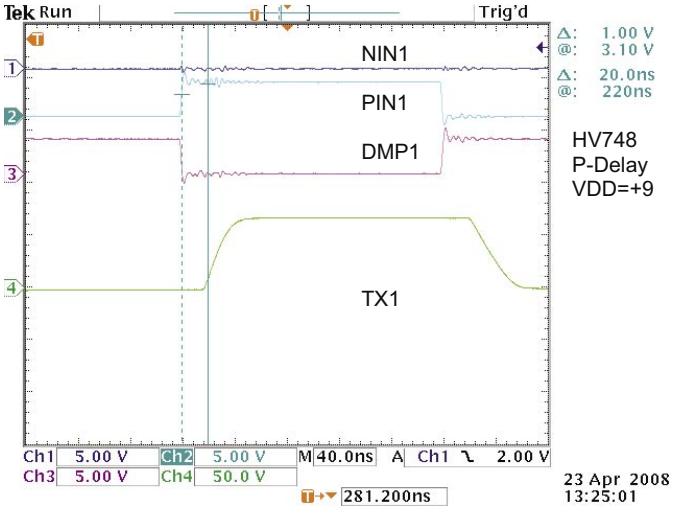


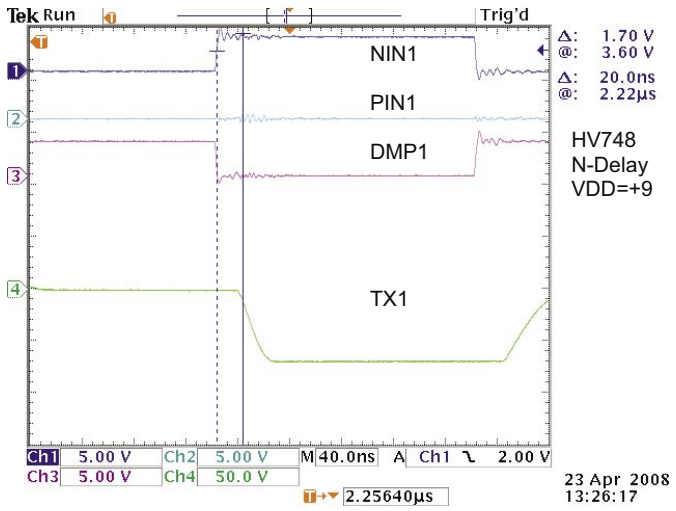


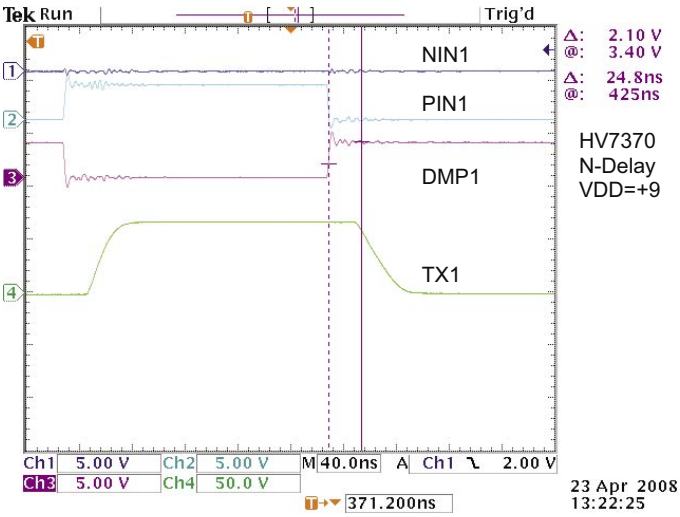
HV7370 RTZ Pulser Waveform Screens *(cont.)*

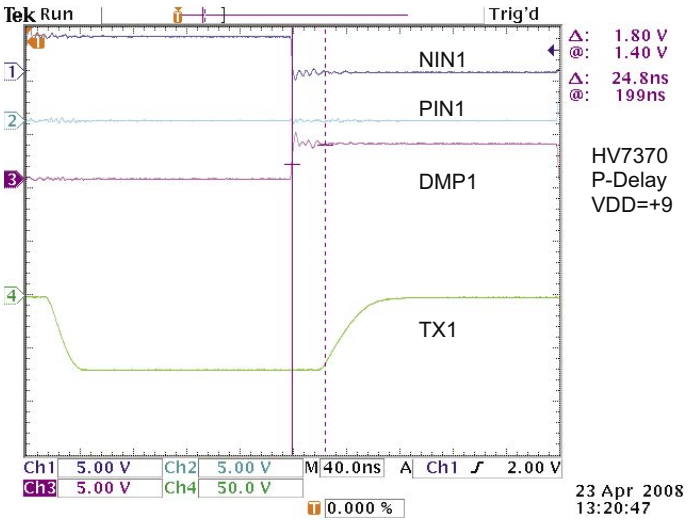




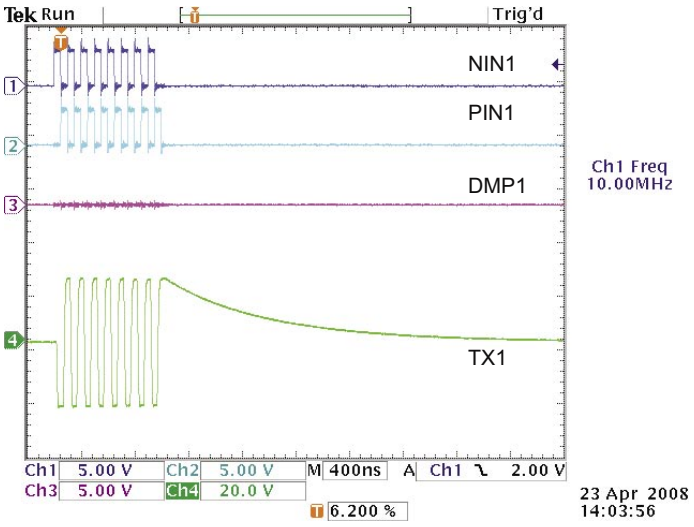


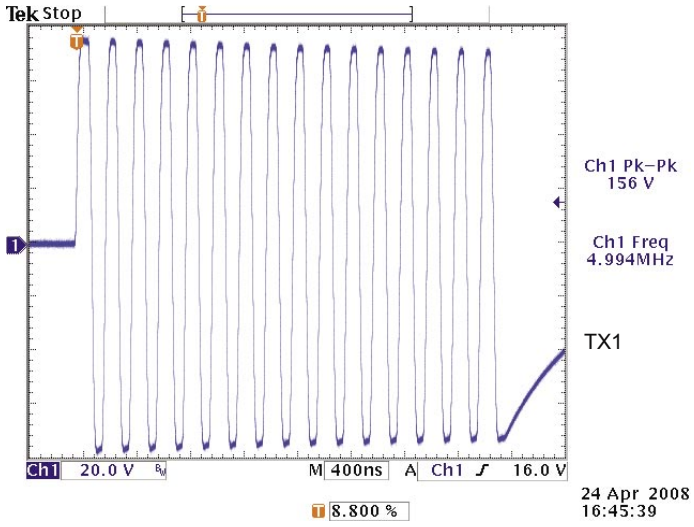


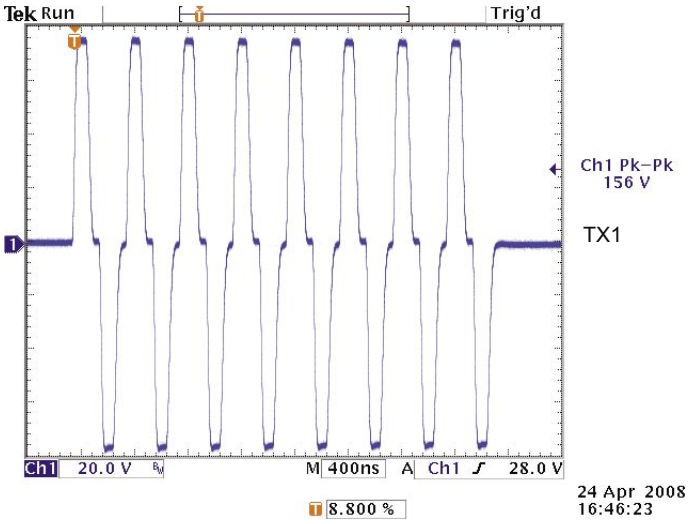


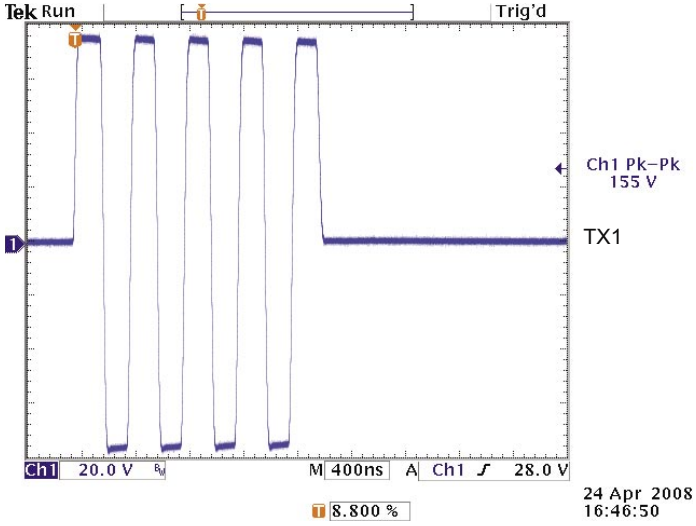


HV7370 RTZ Pulser Waveform Screens *(cont.)*









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