AN 10.15

USB20H04 4-Port USB 2.0 Hub Controller - Layout Guidelines

1 Introduction

This Application Note provides information on designing a printed circuit board (PCB) for SMSC's USB20H04 USB Hub Controller IC. One method will use two layers of copper, while the other will use four layers of copper.

1.1 Two Layer Board Requirements

Designing a PCB with only two layers of copper for the USB20H04 will significantly decrease the cost of building a USB 2.0 Hub. There are, however, more difficulties with routing, controlled impedance, and space when compared to designing a four layer board.

The two layer board example will be built with the following constraints:

- Material: FR-4
- Copper thickness: 1 ounce
- Dielectric Thickness: 31 mils

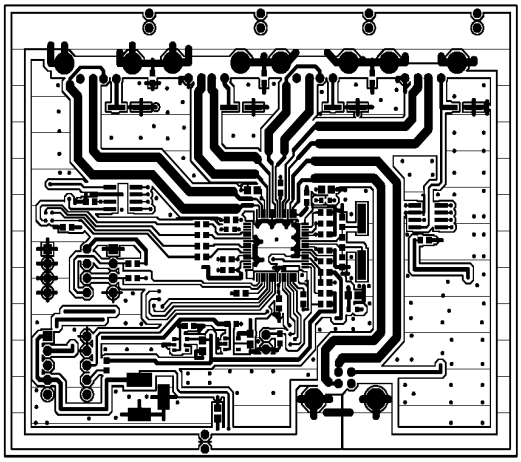

Figure 1.1 Top Layer

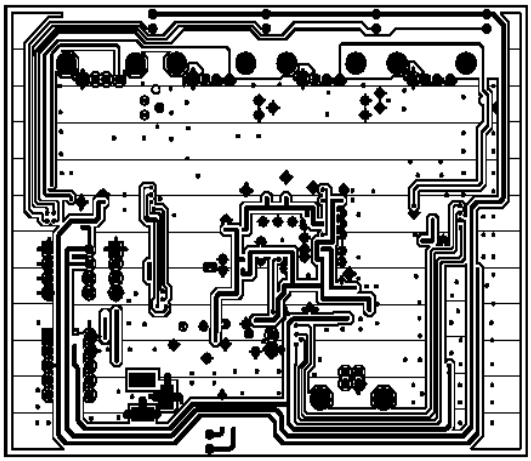

Figure 1.2 Bottom Layer

1.2 Controlled Impedance

The USB 2.0 specification requires that the DP/DM lines maintain a 45 ohm impedance for each trace (90 ohms differential). In order to maintain a 90-ohm differential impedance on the DP/DM lines, there must be a ground plane directly below the differential pair. The ground plane must be uniform, and not broken. Figure 1.2 shows the ground plane below the DP/DM pairs.

The DP/DM lines should be routed with a trace width of approximately 60mils, with 60mils spacing between the two traces. This will make necking down to the pin somewhat difficult, but will allow for the

majority of the track to have a controlled 90 ohm differential impedance. Figure 1.1 shows how the trace must neck down significantly to make contact with the IC pins.

1.3 Crystal Network

The 24MHz crystal should be placed as close to the pins of the USB20H04 as possible. The load capacitors and feedback resistor should also be placed as close to the crystal and IC as possible. It is also recommended that GND not be exposed under the crystal.

1.4 Power Supplies

The VBUS track on the two-layer board must be able to carry enough current to pass the droop test performed by the USB-IF. The droop test requires that there is no more than .330V loss between the IC and the connector. The recommended VBUS track width in ganged mode is 60mils; the recommended VBUS track width in individual port protection mode is 25mils.

The 3.3V supply will be regulated from VBUS (+5V). The 1.8V supply can be regulated from either VBUS or from the 3.3V supply. Refer to Section 3 for power supply requirements.

2 Four Layer Board Requirements

The four layer board example will be built with the following constraints:

- Material: FR-4
- Copper Thickness: 1 ounce
- Overall Board Thickness: 62 mils

The Layer Stack-up will be as follows:

1. Signal Plane
2. GND Plane
3. Power Plane
4. Signal Plane

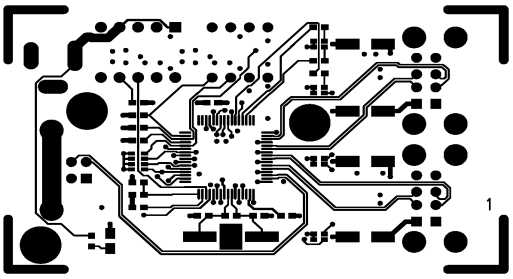

Figure 2.1 Layer 1

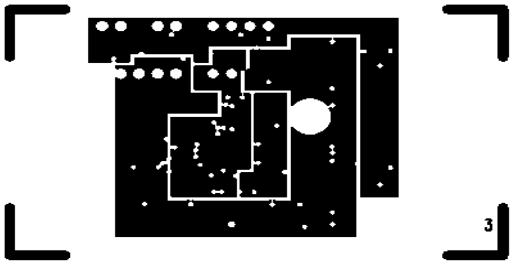

Figure 2.3 Layer 3

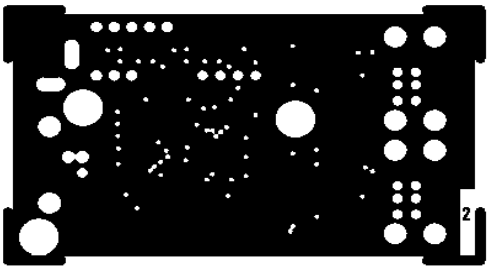

Figure 2.2 Layer 2

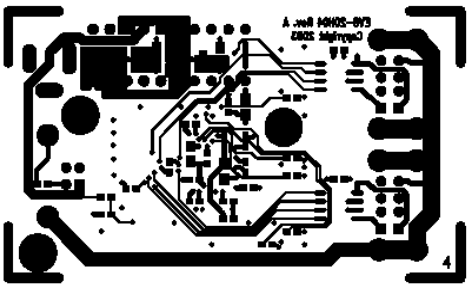

Figure 2.4 Layer 4

2.1 Signal Planes

Figure 2.1 and Figure 2.4 show the signal planes of the 4 layer design.

2.1.1 Controlled Impedance

DP/DM pairs should be routed so that a 90 ohm differential trace impedance (45 ohms single-ended) is maintained. Using the constraints in Figure 2.5 and a trace width and spacing of 10 mils, a 90 ohm differential trace impedance is achieved. The thickness of the FR-4 should be dialed in by the board manufacturer to maintain this desired impedance. The DP/DM pairs should be kept as short as possible, and avoid 90 degree turns and vias if possible.

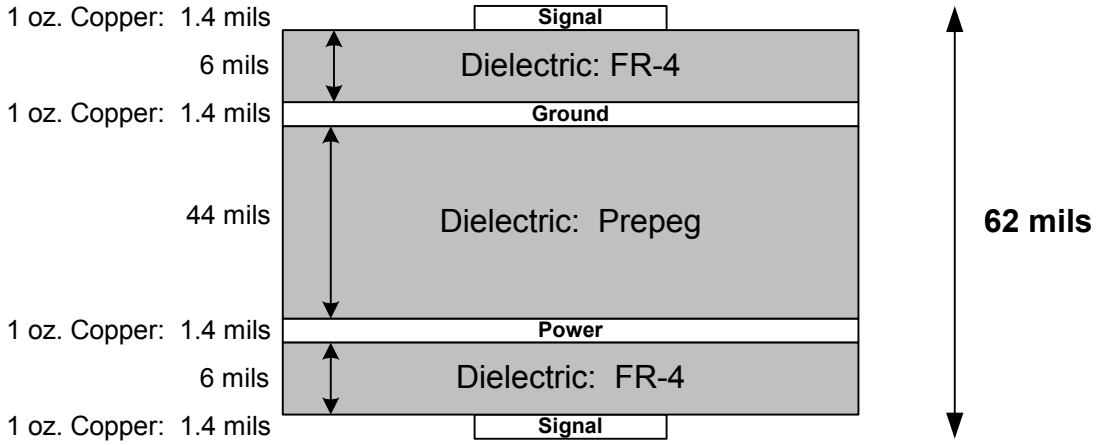

Figure 2.5 4-Layer Stack-Up

2.2 Crystal Network

The 24MHz crystal should be placed as close to the pins of the USB20H04 as possible (preferably directly under the IC at the XTAL pins). The load capacitors and feedback resistor should also be placed as close to the crystal and IC as possible. It is also recommended that GND not be exposed under the crystal.

2.3 Ground Plane

The ground plain will be one solid, undivided plane that will tie all grounds together. It is not necessary to separate analog and digital ground planes if sufficient bypassing is used in the layout.

2.4 Power Plane

The power plane will be divided into four sections: 3.3V Analog, 3.3V Digital, 1.8V Analog, and 1.8V Digital. The 3.3V supplies will be regulated from VBUS (+5V). The 1.8V supplies can be regulated from either VBUS, or from 3.3V. Refer to section 3 for power supply requirements.

3 Power Supply Filtering

This section makes recommendations that will be applied to both 2-layer and 4-layer boards.

3.1 3.3V Supplies

The 3.3V regulator will provide power to both the 3.3V Analog and Digital sections of the power plane. Pins 1,7,13 and 61 will connect to 3.3V Analog. Pin 28 will connect to 3.3V Digital.

A ferrite bead should be placed between the output of the regulator and the 3.3V Analog pins. Panasonic's EXC-3B121H is a suitable ferrite bead for this application.

As shown in Figure 3.1, all of the 3.3V Analog pins will be tied together. A 0.1uF capacitor will be placed as close as possible to each of these pins. Only one 10uF ceramic capacitor is required, and should be placed as close to the group of 3.3V Analog pins as possible. The 3.3V Digital pin only requires a 0.1uF capacitor.

The 3.3V regulator should be able to supply 155mA (this is worst case with four downstream ports active).

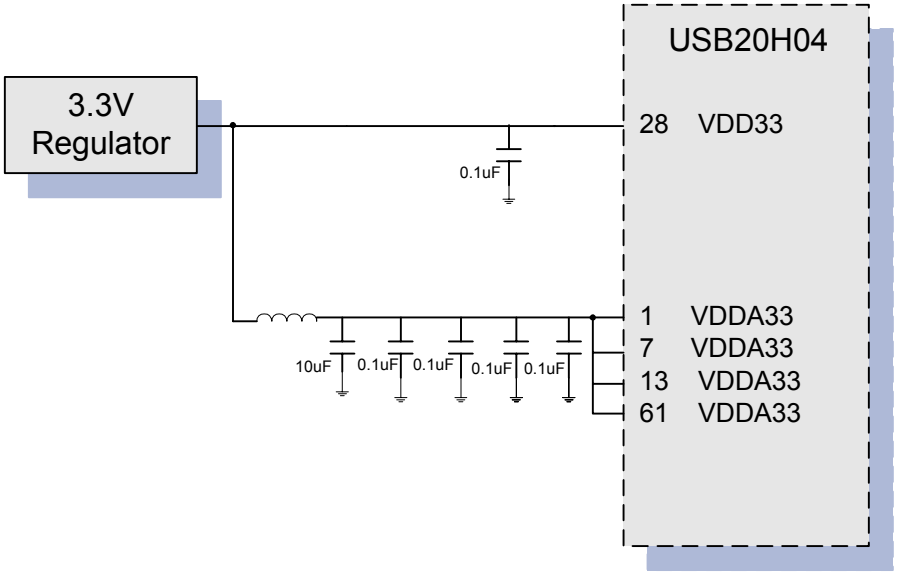

Figure 3.1 3.3V Power Supply

3.2 1.8V Supplies

The 1.8V regulator will provide power to both the 1.8V Analog and 1.8V Digital sections of the power plane. Pins 56 and 60 will connect to 1.8V Analog. Pins 30, 42 and 54 will connect to 1.8V Digital.

A ferrite bead should be placed between the output of the regulator and each of the 1.8V Analog pins. Panasonic's EXC-3B121H is a suitable ferrite bead for this application.

As shown in Figure 3.2, the 1.8V Digital pins will be tied together. A 0.1uF capacitor should be placed as close as possible to each of the 1.8V Digital pins. The 1.8V Analog pins will each require a 0.1uF capacitor and a 10uF ceramic capacitor. These capacitors should also be placed as close as possible to the pins. For low ESR requirements (< 0.1 ohms), it is important that a ceramic 10uF capacitor is used.

The 1.8V regulator should be able to supply 135mA (this is worst case with four downstream ports active).

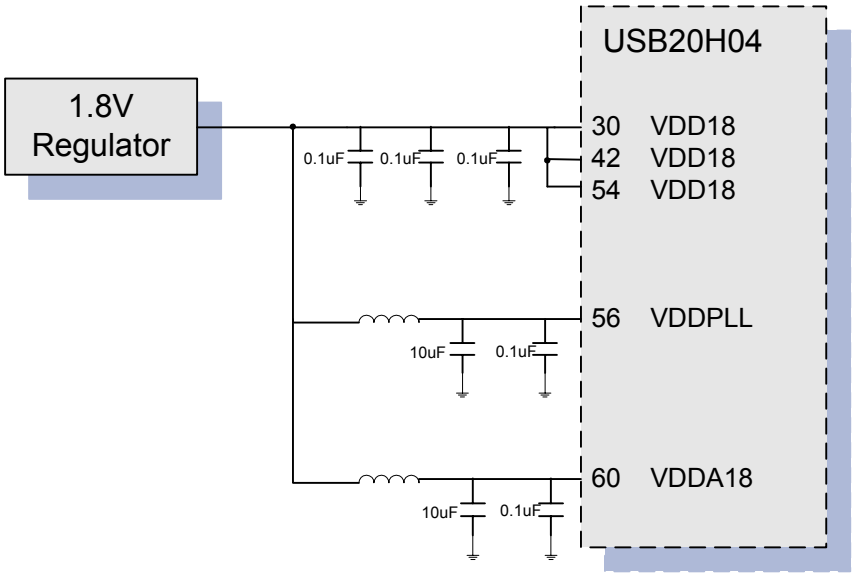

Figure 3.2 1.8V Power Supply

4 ESD Protection

This section makes recommendations that may be applied to both the 2-layer and 4-layer designs.

4.1 Protecting The DP/DM Lines

The USB20H04 is designed to withstand up to 2kV of electro-static discharge (ESD). If more protection on the DP/DM lines is desired, the following devices are recommended:

- Littelfuse: PGB0010603, single line of protection, surface mount suppressor in 0603 package.
- Littelfuse: PGB002ST23, two lines of protection, surface mount suppressor in SOT23 package.
- Littelfuse: PGB0040805, four lines of protection, surface mount suppressor in 0805 package.

The devices listed above do not degrade the AC electrical performance of the USB20H04. Using these devices will increase the ESD tolerance on the DP/DM lines from 2kV to up to 15kV.

4.2 USB Connector Shield

It is recommended that the USB connectors' (both upstream and downstream) shields be decoupled from the GND plane using 0.1uF ceramic capacitors as shown in Figure 4.1 below:

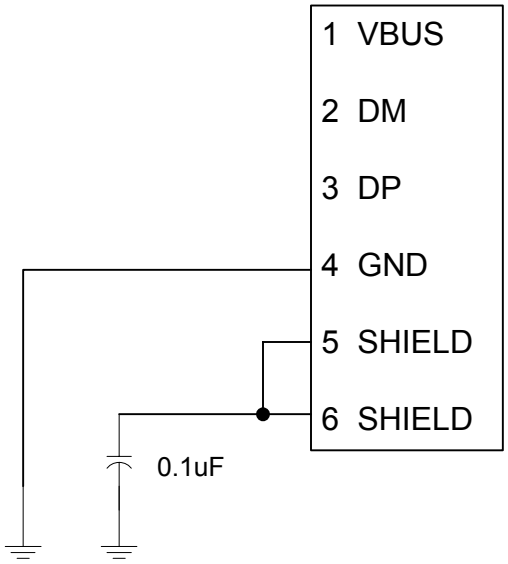

Figure 4.1 USB Shield Decoupling Recommendation

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