Crystal CLoad Selection

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A quartz crystal is a very stable and accurate resonator. However, the accuracy can only be achieved when the crystal is matched properly to the circuit it is used in. Crystal oscillators have a property called “load capacitance” and the crystal needs to be calibrated such that it resonates at its nominal frequency with the desired load capacitance. Voltage controlled crystal oscillators (VCXOs) actually make use of the fact that the crystal resonance frequency changes with the load capacitance of the circuit. By changing the load capacitance between for example 5pF and 20pF, the crystal resonance frequency easily changes with about 400ppm (parts per million).

The formula for the crystal resonance frequency is as follows:

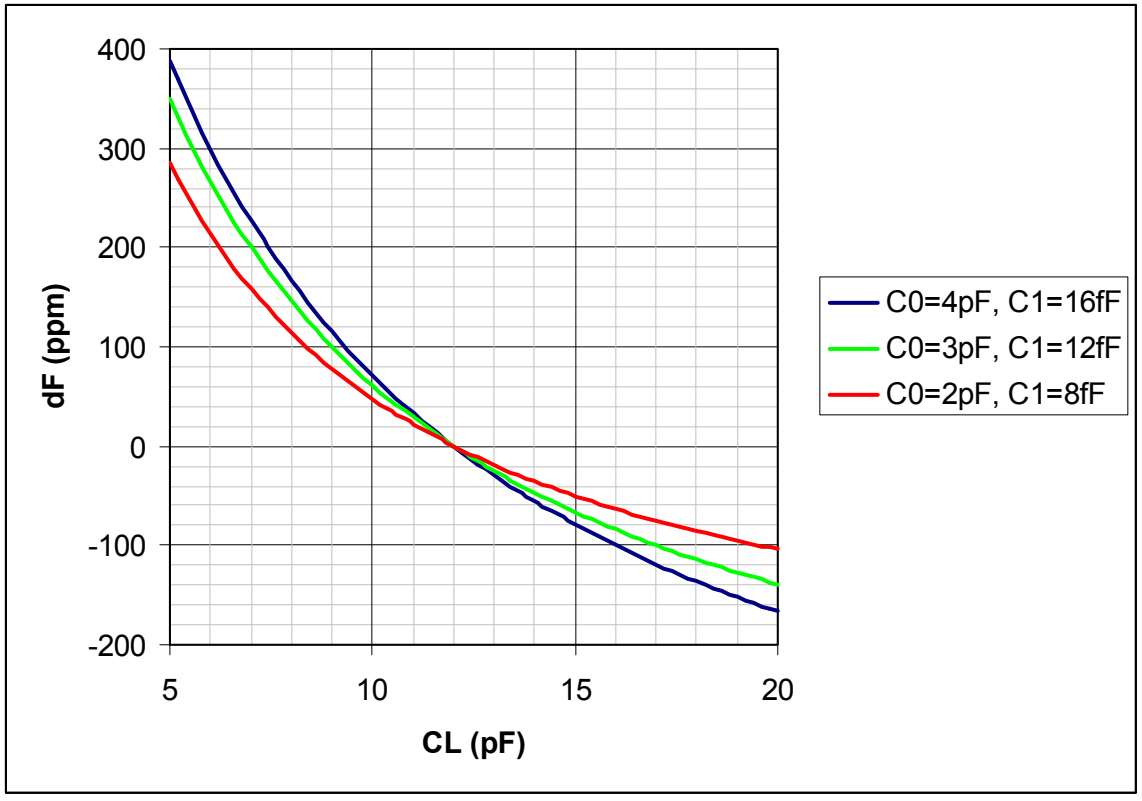
$$Fosc = Fseries \times SQRT(1+C1/(C0+CL))$$

Fseries: The series resonance frequency of the crystal. This is the frequency where the impedance of the crystal is lowest and the phase of the crystal impedance is zero. Rarely crystals are really operated at this frequency. It is only important as a parameter in the crystal behavioral model.
C1: The motional capacitance of the crystal. This is a parameter in the crystal behavioral model that represents elasticity of the quartz material. The larger C1, the more the resonance frequency changes with the load capacitance. This phenomenon is also called “pullability” or “pulling sensitivity”.
C0: The parallel capacitance of the crystal. This simply is the capacitance measured between the two crystal connections. For the most part it is caused by the two electrodes on the quartz plate and another small part is from the crystal housing.
CL: This is the circuit “capacitance” as seen between the two crystal connections.
Fosc: The resonance frequency of crystal as a function of the above parameters. This will be the frequency where the crystal oscillator will operate.

This paper will concentrate on the load capacitance CL and its influence on the crystal oscillator frequency. Lets start with an example to illustrate the impact of a small CL error:

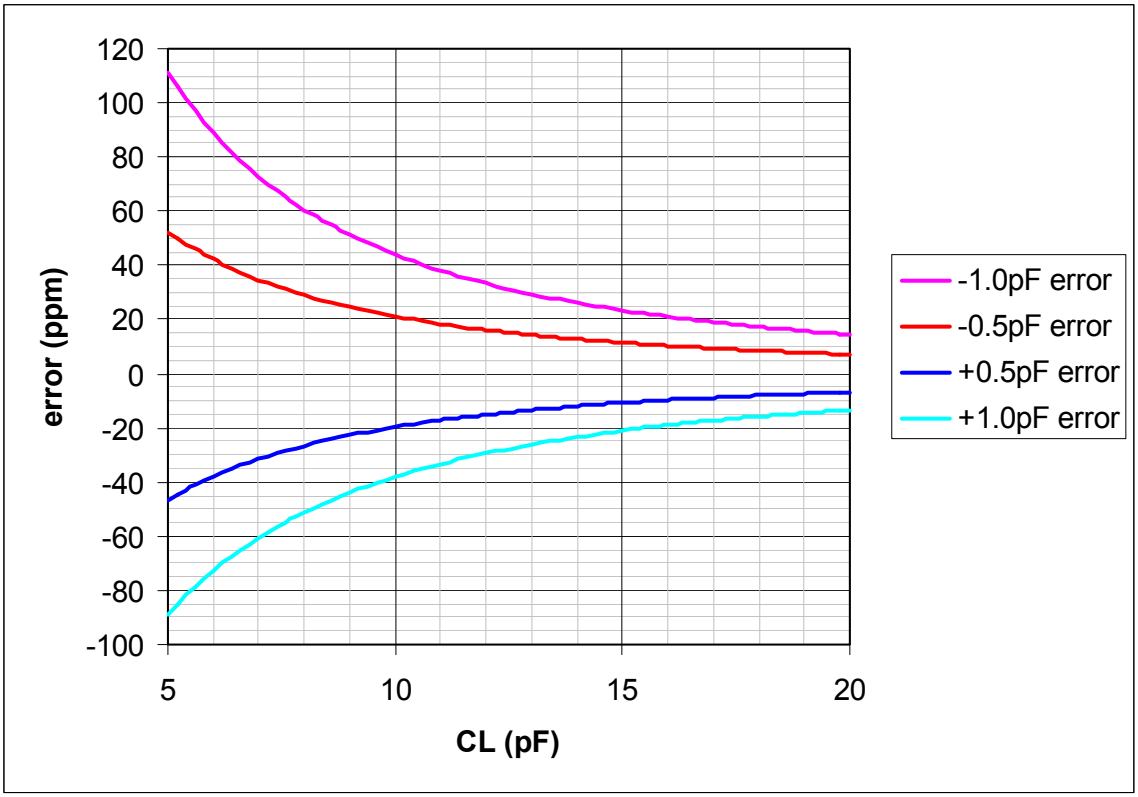
Lets assume a typical fundamental mode crystal with C0=4pF and C1=16fF. Lets assume the crystal was calibrated to resonate at the nominal frequency with CL=12pF. However, the circuit has a bit more parasitic capacitance than expected and the CL turns out to be 13pF instead.
At CL=12pF: Fosc = Fseries × SQRT(1+0.016/(4+12)) = Fseries × 1.000,500
At CL=13pF: Fosc = Fseries × SQRT(1+0.016/(4+13)) = Fseries × 1.000,471
At CL=12pF the crystal oscillator will run 500ppm above the series resonance frequency of the crystal and at CL=13pF the crystal oscillator will run at 471ppm above the series resonance frequency of the crystal. So as a result of the 1pF error in CL, the crystal oscillator will be running 29ppm lower than intended. If the application requires 100ppm accuracy and the crystal is specified to be within 50ppm, you may not care about this offset. But if the application requires better frequency accuracy and you need to match crystal and circuit within for example 10ppm, then it is necessary to pay extra attention to the exact CL value.

Below graph shows the relation between the crystal oscillator frequency and the CL value.



Three different crystals, each with different properties were used for this plot. As you can see the different crystals show different sensitivity to CL change. You can also see that the sensitivity is much higher when the CL value is small because the line is steeper. It means that a 1pF error with a 5pF nominal CL will have a much bigger impact on frequency than a 1pF error with a 20pF nominal CL.

Below graph shows the frequency error from a 0.5pF and 1pF CL error.

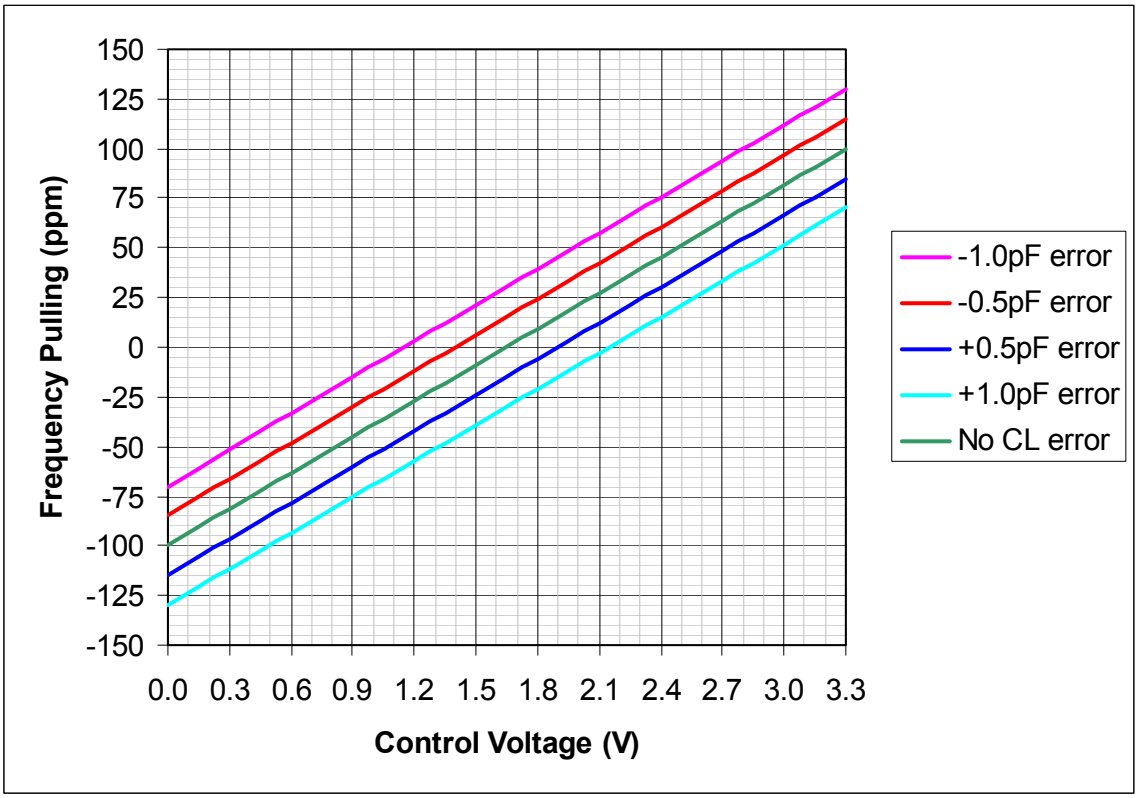


The crystal with C0=4pF and C1=16fF was used for this graph.

As an IC manufacturer we can really only address the CL contribution of the IC itself. It will of course be the main contribution but the influence of the traces and solder pads connected to the crystal and IC crystal connections should not be underestimated.

Consequences of CL errors

With a simple clock oscillator it is easy to understand that the frequency tolerance budget will be reduced with the frequency error caused by the CL error. With a VCXO it is essentially the same although less easy to understand. VCXOs are mostly used to lock to a reference frequency source. When there is a CL error the VCXO may still lock and the frequency does not change. However, the control voltage for the VCXO to achieve the reference frequency has changed. Below graph tries to illustrate what happens with a CL error in a VCXO circuit:



The green "No error" line is the ideal situation. The frequency passes through zero at the mid control voltage of 1.65V. The frequency can pull 100ppm down and up from the center. Lets assume the application requires at least 50ppm of pulling around the ideal reference frequency. This is called "50ppm APR" (Absolute Pulling Range). The additional pulling reserve is to be able to correct for component tolerances or frequency variations due to environmental variations (temperature, power supply, ….).

For example, when the CL error is +1pF, the circuit moves the control voltage to about 2.1V to maintain the reference frequency. You can see in the plot that the remaining pulling above the reference is now only 70ppm. This means that the original reserve of 50ppm for tolerances and variations has shrunk to 20ppm. Most likely this is not enough and there will be a significant amount of products that will fail close to extreme conditions. In a dynamic circuit where the control voltage will move to maintain the reference frequency, it may be important to check that the control voltage is close to the center of its range under nominal environmental conditions.

Trimming the circuit

One way of dealing with a certain level of uncertainty in the total CL of the circuit is to add a capacitor in series with the crystal. Lets say the crystal is calibrated to 12pF and the circuit capacitance (without series capacitor) is about 14pF, then the series capacitor needs to be 84pF to match the circuit to the crystal. If you made a 1pF error like above and the circuit is actually 15pF, then a series capacitor of 60pF is needed. A 1pF error in the opposite direction, to 13pF, requires a series capacitor of 156pF. Generally speaking, if you do not know the exact CL value but you know it is within the 13~15pF range, then you can simply find a series capacitor value that brings the average crystal oscillator frequency closest to the desired target.

This method is most suited for clock oscillators (XOs). You have to be a bit careful using this method with a VCXO. The VCXO is already changing the capacitance on the chip to pull the frequency. Adding another capacitor in series will change the frequency pulling characteristics a little bit. The overall pulling range will decrease a little bit. It will actually decrease the pulling more on the low side of the frequency pulling range so pulling linearity may be affected also. In above example, 156pF in series will have almost no influence on most VCXO circuits. However, 60pF will be noticable…..

Customizing the crystal

Making a quartz crystal suited for operation with a certain CL value is a matter of frequency finetuning at the end of the crystal manufacturing process. The crystal manufacturer will apply the same CL to the crystal during this frequency finetuning as the CL value of the crystal oscillator circuit. History shows however that crystal oscillator circuits are never exactly 12.000pF for example and it will be difficult to find a crystal "off the shelf" that will operate at the exact right frequency. The crystal manufacturer could customize the CL with the following procedure:

1) Get a few crystals from the crystal manufacturer (5 or 10) of the correct model, the correct frequency and a CL value close to where you expect the oscillator circuit to be.
2) Use each crystal in 5 or 10 of the intended crystal oscillator circuits and record the average frequency observed for each crystal.
3) Send the crystals back to the crystal manufacturer with the list of frequencies observed for each crystal.
4) The crystal manufacturer will now use these crystals as a reference to calibrate a customized load capacitance for this crystal oscillator application.

This method uses the fact that when a certain crystal runs at the same frequency in both the crystal oscillator application and the crystal frequency finetuning machine, both CLs have to be identical. Step 3 may not be necessary if the crystal manufacturer noted exact crystal parameters before they were sent to the customer. Then it may be sufficient to just tell the crystal manufacturer at what frequency each crystal is running.

CL values for several PhaseLink ICs:

Below values are for the IC only and do not include additional capacitance for the PCB layout.

Partnumber	**Conditions**	**Load Capacitance**
PLL500-17SC	VCON = 1.65V	7.8 pF
PLL500-37SC	VCON = 1.65V	5.1 pF
PLL502-3xOC	VCON = 1.65V	8.7 pF
PLL502-51SC	VCON = 1.65V	9.8 pF
PLL520-0xOC	VCON = 1.65V	4.8 pF
PLL520-3xOC	VCON = 1.65V	5.5 pF
PLL520-47OC	VCON = 1.65V	5.5 pF
PL521-23OC	VCON = 1.65V	4.9 pF
PL560-3xOC & -4xOC	VCON = 1.65V	4.9 pF
PLL600-27OC		7.7 pF