

SAW DEVICES

GLOSSARY OF TERMS

Nominal frequency (Fn): The nominal values of the center frequency F_0 and is used as the reference frequency of related standard. Unit of nominal frequency is in MHz.

Insertion Loss (IL): The logarithmic ratio of the power delivered to the load impedance before the filter is inserted to the power delivered to the load impedance after the filter is inserted. Unit of Insertion loss is in dB.

Pass Bandwidth (BWp): The frequency interval in which the relative attenuation (the attenuation from the minimum insertion loss) is equal to the specified value 3dB.

Stop Bandwidth (BWr): The frequency interval in which the relative attenuation (the attenuation from the minimum insertion loss) is equal to the specified value of "A" dB.

Group Delay Ripple (GDR): The difference between the maximum and minimum value of the group delay in the specified range of the pass band. Unit in μ s.

Pass band Ripple (AR): The difference between the minimum peak attenuation and the maximum peak attenuation within a pass band. Unit is in dB.

Terminating Impedance (Zt): Impedance presented to the filter by the source or by the load.

HANDLING PRECAUTIONS

1. Use the SAW product within its maximum ratings.
2. Never apply voltage higher than the maximum rating since high level voltage could accelerate deterioration of the SAW characteristics.
3. The shield grounding condition should be determined so that electrical coupling between input and output may be minimized before using the device. Coupling between input and output will cause ripples in the pass band amplitude and group delay.
4. Storage temperature shall not exceed 85°C.
5. Be careful when using ultrasonic cleaning SAW products since device material and construction is sensitive to ultrasonic vibration.
6. Do not apply sudden or excessive thermal or mechanical shock to the SAW products since it could worsen or deteriorate the SAW characteristics.

ENVIRONMENTAL AND MECHANICAL SPECIFICATIONS

Shock (Drop test): Natural drop on a hardwood board at 1.0m, 3 times. The specimens shall meet the electrical specifications.

Vibration: Frequency with an amplitude of 1.5mm sweeping between 10Hz to 55Hz within 1 minute for 2 hours minimum on each axis on three (3) mutually perpendicular axes. The specimens shall meet the electrical specifications.

Resistance to solder heat: Immerse the leads or terminals in soldering bath at 245° \pm 5°C for 5 \pm 0.5 s. 75% or more of the immersed surface shall be covered with solder.

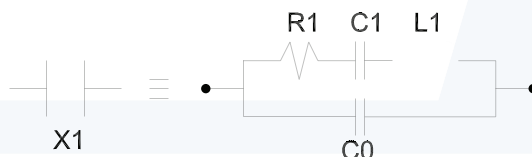
Temperature characteristics: Specimens shall be measured within -40°C to +85°C temperature range. The specimens shall meet the electrical specifications.

Dry heat (aging test): Temperature 125°C \pm 2°C for 250 hours. The specimens shall meet the electrical specifications.

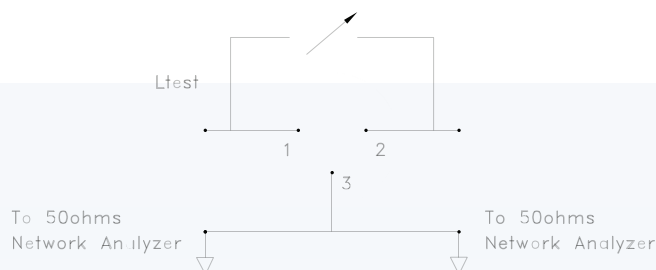
Cold resistance: Temperature - 40°C \pm 3°C. Duration 96 hours. The specimens shall meet the electrical specifications.

Thermal shock: Heat cycle conditions -55°C (30 minutes), 25°C (5 minutes), +85°C (30 minutes) for 5 cycles. The specimens shall meet the electrical specifications.

EQUIVALENT LC MODEL SAW RESONATOR



TEST CIRCUIT SAW RESONATOR



SAW DEVICES

Definition of SAW:

Surface Acoustic Wave (SAW) is a wave propagating along the surface of an elastic substrate. Frequency of SAW is:

$$F = \frac{V}{\lambda}$$

Where V is the velocity of SAW (~ 3,100m/s)

λ Is the IDT period.

Frequency range of SAW products is 10MHz to 3GHz.

SAW filters characteristics:

- ◆ SAW filter is an integrated, passive device with bandpass filter characteristics.
- ◆ Operation is based on the interference of mechanical surface waves.
- ◆ Input/Output transducers are formed on a piezoelectric material.

SAW filters advantages:

- ◆ Reduced size and weight.
- ◆ High reliability and ruggedness.
- ◆ No tuning or readjustment.
- ◆ Mass production capable.

SAW filters fundamentals:

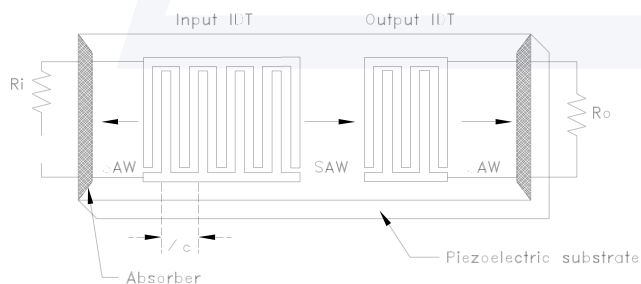
SAW devices consist of two transducers with interdigital transducers of thin metal electrodes deposited on a piezoelectric substrate such as quartz or lithium tantalite. One of these acts as the device input and converts signal voltage variations into mechanical surface acoustic waves. The other IDT is used as an output receiver to convert mechanical SAW vibrations back into output voltages. Such energy conversions require the Interdigital transducers to be used in conjunction with elastic surfaces that

SAW filters manufacturing process:

- ◆ Wafer (LiTaO₃ or LiNbO₃, or SiO₂)
- ◆ Al deposit (sputtering) 0.15μ to 1.5μ
- ◆ Photoresist (PR coating)
- ◆ Exposure
- ◆ Develop
- ◆ Al etching (Wet etching)
- ◆ PR removal
- ◆ QC check + Probing (F0, IL)
- ◆ Sieving (Scribing)
- ◆ QC check (chips, cracks)
- ◆ Mounting Ag/UV bond
- ◆ Wire bonding
- ◆ Seam sealing
- ◆ Marking
- ◆ Final tests and inspections

SAW filter parameters:

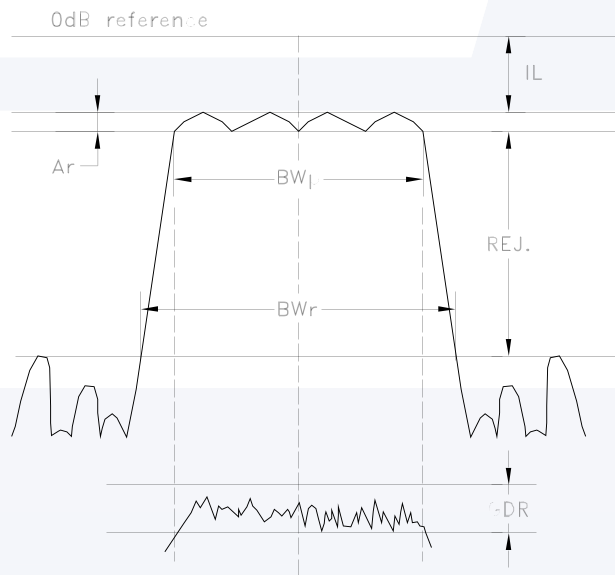
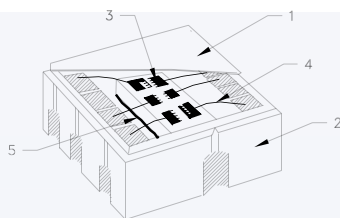
- * Nominal frequency Fn (MHz)
- * Pass Bandwidth 3dB BWp (MHz)
- * Stop Bandwidth BWr (MHz)
- * Insertion Loss IL (dB)
- * Pass Band Ripple AR (dB)
- * Group Delay GD (μs)
- * Temperature coefficient TC (ppm/K)
- * Termination Impedance (ohms)
- * Operating temperature range T (°C)



are also piezoelectric ones.

SAW devices structure:

No.	Parts list	Materials
1	Lid	FeNiCo
2	Ceramic base	Al2O3
3	Chip (Die)	LT, LN, SiO2
4	Wire	Al, Au



QUARTZ CRYSTAL GLOSSARY OF TERMS

Nominal frequency: The specified center frequency of the crystal. Unit of frequency is Hertz (Hz). Quartz crystals are specified in kHz or MHz.

Crystal equivalent circuit: The crystal equivalent circuit of the quartz crystal consists of a motional capacitance C1, the motional inductance L1, a series resistance R1, and a shunt capacitance C0. The first three parameters are known as the “motional parameters”. See figure 1.



Operating mode: The quartz crystal could operate at its Fundamental mode or harmonic modes. The fundamental mode is always the preferred oscillating mode. Odd harmonics such as 3rd, 5th, 7th, etc. are overtone modes.

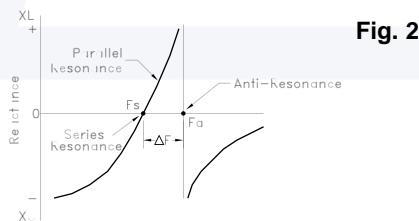
Frequency tolerance: The maximum allowable frequency deviation from a specified nominal frequency at ambient room temperature (25°C ± 3°C). Frequency tolerance is expressed in percent (%) or parts per millions (ppm).

Frequency stability: The maximum allowable frequency deviation from the ambient temperature over the temperature range. Frequency stability is expressed in percent (%) or parts per millions (ppm). The frequency stability is determined by cut type, angle cut, angle cut tolerance, mode of operation, package styles, and mechanical dimensions of the quartz blank.

Series vs. Parallel resonance: When a crystal is operating at series resonance (Fs), it looks resistive in the circuit. At this point $X_L = X_C$. In series resonance, load capacitance does not have to be specified. The antiresonant frequency (Fa) occurs when the reactance in the series branch is equal to C0.

When a crystal is operating at parallel resonance, it looks inductive in the circuit. The crystal equivalent circuit can be simplified as a series resistance Re with a reactance Xe.

The difference in frequency between the Fs and Fa depends on the C0/C1 ratio of the crystal unit, and the inductance L1. In parallel resonance, the load capacitance shall be specified.



Equivalent Series Resistance (ESR): The value of impedance the crystal exhibits in the operating resonant circuit.

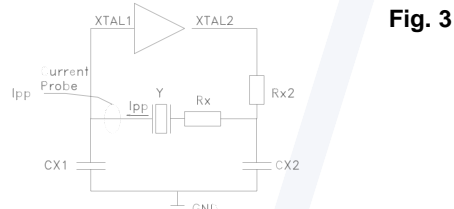
Aging: The relative frequency change over a certain period of time and is typically expressed as a maximum value in parts per million per year (ppm/year). Typically, aging is computed within the first 30 days to 90 days and predicted exponentially over a longer period usually a year.

Operating temperature: The minimum and maximum temperatures within which crystal unit operates under specified conditions.

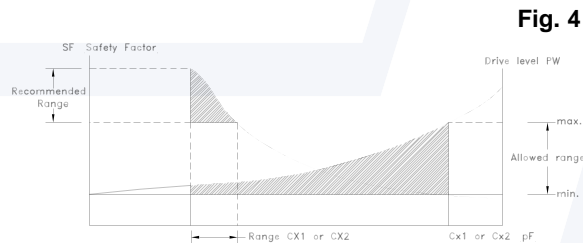
Storage temperature: The minimum and maximum temperatures that the crystal unit can be safely stored.

Drive level: A function of the driving or excitation current flowing through the crystal. The drive level is the amount of power dissipated in the crystal and is expressed in milliwatts or microwatts. Drive level should be kept at a safe minimum condition to assure proper start-up. Excessive drive level will result in possible long-term frequency drift or crystal fracture.

Figure 4 shows the relationship between drive level and circuit load



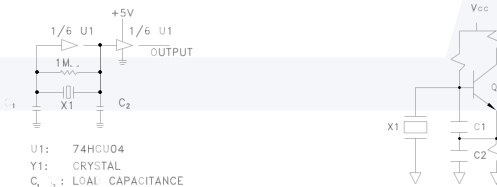
capacitance and optimum value guarantee for start-up condition.



Load capacitance: Load capacitance (CL) is the amount of capacitance that the oscillator exhibits when looking into the circuit through the two crystal terminals. Load capacitance needs to be specified when the crystal is used in a parallel mode. Load capacitance is calculated as follows:

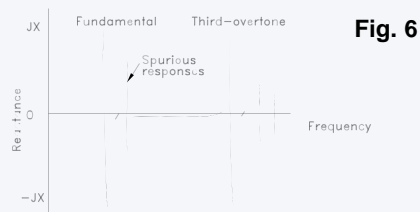
Pierce circuit

Colpitts



$$CL = \frac{(C1 \times C2)}{(C1 + C2)} + C_{stray}$$

Spurious responses: Unwanted resonance usually above the operating mode, specified in dB max. or number of times of main mode ESR value. Frequency range is specified within couple of hundreds kilohertz.



QUARTZ CRYSTAL GLOSSARY OF TERMS

Crystal cuts: A blank wafer is obtained by cutting the quartz bar at specific angles to the various axes. The choice of axis and angle cut determines the physical and electrical parameters of the resonator. Figure 7 shows combinations of X, Y, and Z rotational cuts which are labeled in industry as AT, BT, CT, DT cut, etc. The most two common cuts in Abracon crystals are AT and BT-cuts. There are differences in temperature coefficients of the two cuts.

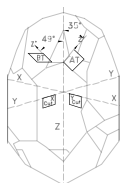


Fig. 7

Vibration modes: The crystal vibrates and produces a steady signal when it is excited with a voltage. The mode of vibration depends on crystal cuts such as thickness shear for AT and BT cuts, length-width flexure for tuning fork, Face shear for CT, DT cuts, etc. Figure 8 shows a thickness-shear mode.

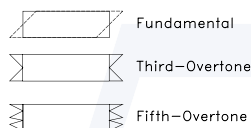


Fig. 8

Shunt capacitance C0: The static capacitance between the electrodes (Ce) together with holder capacitance (Ch).

$$C_0 = C_e + C_h$$

Ch varies between 0.6pF to 0.8pF depending on mounting method.

Motional capacitance C1: The capacitance of the nominal arm of the equivalent circuit. C1 results from the elasticity of the quartz blank.

$$C_1 \text{ (pF)} = 0.22 \times A \text{ (m}^2\text{)} \times F \text{ (Hz)} / 1670$$

Where A = area of electrode in m²

Quality factor Q: The factor that represents the sharpness of the resonant curve. Quartz crystal has a very high Q compared to other resonators typically in 10,000 to 100,000s.

$$Q = \frac{2 \cdot \pi \cdot F_s \cdot L_1}{R_1} = \frac{1}{2 \cdot \pi \cdot F_s \cdot C_1 \cdot R_1}$$

Pullability: When a crystal is operating at parallel resonance, it looks inductive in the circuit. As the reactance changes, the frequency changes correspondingly, thus change the pullability of the crystal. The difference in frequency between the Fs and Fa depends on the C0/C1 ratio of the crystal unit and the load capacitance CL.

Delta F from series resonant to parallel resonant in ppm:

$$\frac{FL - F_s}{F_s} = \frac{\Delta F}{F_s} = \frac{C_1}{2(C_0 + CL)}$$

Pullability can be expressed in terms of load sensitivity (TS) in ppm/pF.

$$TS \text{ (ppm/pF)} = \frac{10^6 \cdot C_1}{2(C_0 + CL)^2}$$

Negative resistance (-R): Negative resistance is used to evaluate circuit oscillation allowance. Lack of negative resistance could lead to initial circuit start-up and and unstable oscillation at steady state.

Procedure:

1. Connect the external resistance Ri in series with the crystal.
2. Adjust Ri value until oscillation stops.
3. Record Ri value.
4. Negative resistance -R = Ri + R1
5. Recommended - R value to be at least 5 to 10 times greater than Re.

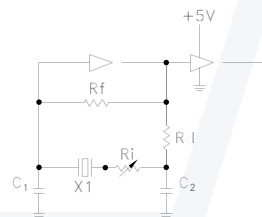


Fig. 9

See figure 9.

Frequency vs. temperature characteristics: Figure 10 shows the frequency – temperature characteristics for a thickness-shear AT cut crystal. The AT-cut curve has an S-shape symmetrical to room temperature.

Quartz crystals manufacturing process: Quartz crystals are

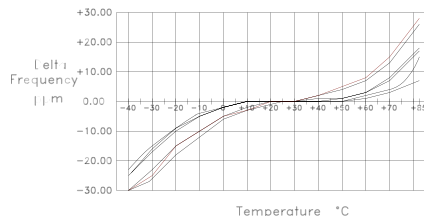


Fig. 10

manufactured in a clean environment to assure high-precision. Highlights of the major steps in manufacturing process of the AT-Cut crystal are described below:

- As grown quartz bars – Lumbering – Cutting – Measurement of angle – Precision lapping – Beveling – Etching and Cleaning – Base coating – Mounting – Fine frequency adjusting – Annealing – Sealing – Aging – Final tests and Inspections.

Crystal mounting methods: Quartz blank unit is mounted on holder mounts with conductive epoxy or solder (tuning fork). Precise amount of silver epoxy is applied with automounter

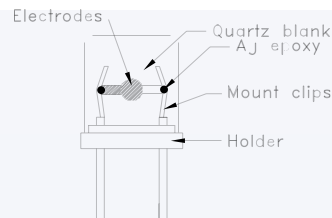


Fig. 11

QUARTZ CRYSTALS

The following considerations must be well studied in order to select the right crystal for your applications:

1) ASIC CHARACTERISTICS:

- Negative resistance.
- Small-signal gain analysis.
- Input and output resistance.
- Propagation delay between input and output of inverter.
- Gain-phase analysis.
- Supply voltage operational margin.
- Circuit configuration.
- Feedback resistor value (if integrated within the ASIC).
- Built-in load capacitance on X1 and X2 ports.
- Sensitivity of inverter operation versus stray inductance or capacitance due to layout or attachment methods.

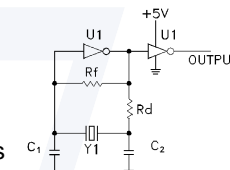
2) CRYSTAL CHARACTERISTICS:

- Mode of Operation (Fundamental -vs.- Overtone).
- Series -vs.- Parallel.
- If Parallel: State "Load Capacitance".
- If Overtone: specify design without inductor or conventional tuning tank LC Circuit.
- Maximum Resistance.
- Drive Level dependency.
- Operating Temperature.
- Frequency Accuracy at 25°C.
- Frequency Stability over Temperature.
- Aging.
- Pulling Characteristics.
- Spurious Responses.

3) CIRCUIT CONSIDERATIONS:

- **Select the best value for Rf (feedback resistor).**
Recommend Value:
Low kHz Range: between 10 MΩ to 20 MΩ
MHz Range: between 100kΩ to 1 MΩ
- **Select Series Resistance Value (Rd) for impedance matching.** Rd selection varies with ASIC negative resistance, output resistance and load impedance. Typical Value for Rd: 0Ω (Short) to 1kΩ from 4 MHz to 30 MHz.
- **Study the Voltage Gain from output to input $V_i / V_o = C_2 / C_1$.** It is very common to select equal values of C1 and C2 in the circuit, but sometimes it is necessary to make the output load capacitance (C2) higher to compensate for the signal losses through the crystal and feed back loop.
- **Maximum Crystal Resistance Allowed.** Low resistance is desirable for better operational margin and stability. However, crystal resistance varies with frequency, blank size. Low crystal resistance could affect yield and therefore cost.
- **Typical Crystal Aging: ± 5 ppm per year maximum.** Aging over 10 years: ± 10 ppm to ± 15 ppm maximum. Tighter aging (up to ± 1 ppm per year max.) is available. Tighter aging requires extremely high design, manufacturing and additional post-tests.
- **Inductorless Third (3rd) Overtone:** The Inductorless 3rd-Overtone circuit is similar to the fundamental

frequency circuit except the feedback resistor value is made much smaller (typical value varies between 2 kΩ to 6 kΩ). In this case, the component of inductive admittance due to the resistor is greater than the admittance of the loading capacitance at the fundamental frequency, thereby preventing oscillation at the fundamental frequency. In the meantime, the inductive admittance at the overtone is less than the admittance of the Load Capacitor thus enabling the oscillation at the third-overtone. (See figure 1.)



U1: ASIC
Y1: Crystal
C1 C2: Load Capacitance

Figure 1

Tuning Tank LC Overtone Circuit

- In an overtone mode, an additional inductor L1 and capacitance Cc is required to select the 3rd-Overtone mode, while suppressing or rejecting the fundamental mode. Choose Lc and Cc component values in the 3rd-overtone crystal circuit to satisfy the following conditions:
- The Lc / Cc component form a series resonant circuit at a frequency below the fundamental frequency, which makes the circuit look inductive at the fundamental frequency. This condition does not favor to oscillation at the fundamental mode.
- The L1 / Cc and C2 components form a parallel resonant circuit at a frequency about half-way between the fundamental and 3rd-Overtone frequency. This condition makes the circuit capacitive at the 3rd-Overtone frequency, which favors the oscillation at the desired Overtone mode. (See figure 2).
- The Lc tank may be located at either input or output of the inverter. However, the Lc tank at the out put is referred, because it helps to clean up all unwanted modes before signal goes through the crystal.

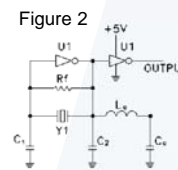
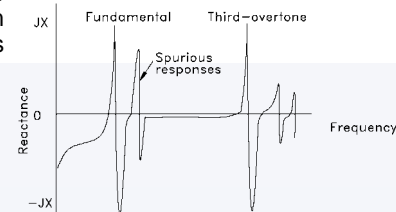


Figure 2

4) CONTROL UNWANTED MODES IN CRYSTALS:

Unwanted modes are resonant modes in addition to the desired modes (Fundamental, Third-Overtone, Fifth overtone, etc.). The frequencies of these unwanted modes are usually slightly higher than the desired modes within couple of hundreds kilohertz. In oscillator applications, it is necessary to control unwanted modes as lower as possible to prevent circuit oscillating in the "spurious mode". See Figure 3. The design of large electrodes on crystal to produce large pulling is a common cause of promoting spurs. Unwanted modes are usually specified in terms of resistance or in terms of the ratio of resistance of the unwanted mode to the resistance of the main mode over a bandwidth of desired frequency. A resistance ratio of 2:1 or a minimum of 3dB separation is usually adequate.



QUARTZ CRYSTALS

Q: Why does my crystal works sometimes, but not others?

A: This is the most common complaint heard from crystal users. Unless the crystal supplier knows this common mode of failure, and applies preventive measures, this common problem can be solved earlier in design stage. Some customers describe these crystals as “sleeping crystals”. The circuit start-up sometimes and does not at other times, unless been touched with a scope probe or fingers. Abracon predicts this problem in our Design and Process Failure Mode Effect Analysis (DFMEA and PFMEA) with two main root causes:

- Blank cleanliness.
- Drive level dependency.
- IC matching.

• Blank cleanliness: We use special blank wafer ultrasonic cleaning procedure in De-ionized water and 99.99% Isopropyl Alcohol with modulated air method to guarantee highest quality.

• Drive level dependency: On most production lots, we perform 100% DLD tests at five levels minimum starting from 1μW to 500μW. The DLD test will guarantee that the changes in ESR and frequency are within maximum limits thus assure the initial power start-up.

Typical ΔFDLD: ± 5ppm max.
Typical ΔRDLD: 25% max.

• IC matching: Abracon offers IC matching process to our customers in early design stage. The IC matching process will identify the optimum values of load capacitors, feedback and series resistors, drive level vs. load cap, voltage margin, open-loop gain at resonance, and temperature characteristics. Please consult Abracon for details.

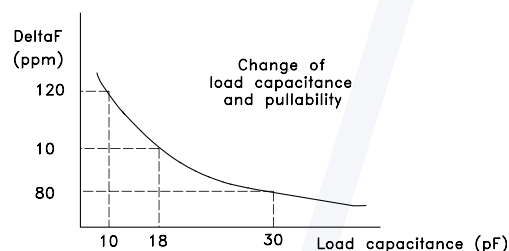
Q: How to specify a pulling crystal?

A: Many applications in VCXO, PLL network require a crystal with pulling characteristics. The pullability of the crystal can be explained as follow:

When a crystal is operating at parallel resonance, it looks inductive in the circuit. As the reactance changes, the frequency changes correspondingly, thus change the pullability of the crystal. The difference between the Fs and Fa depends on the ratio C0/C1 ratio of the crystal.

The following crystal parameters specify the pullability:

- Motional capacitance C1 in fF.
- Motional inductance L1 in mH
- The difference of the parallel resonant frequency $\Delta F = FL2 - FL1$



- Ratio of shunt capacitance to motional capacitance C0/C1. The smaller ratio the better the pulling.

The pullability of the crystal can be designed to meet customer's requirements. However, the pulling function varies with package size, electrode size, frequency, load capacitance range, and operating mode. Please contact Abracon whenever you have a need for a pulling crystal.

Q: What is the trend of crystal packaging and advantages?

A:

- Minimizing the size and weight of mobile communication application such as cellular phones, PCMCIA, PDA, etc.
- Improve sealing technologies from resin sealing to seam sealing to Electron beam sealing.
- Advanced small quartz blank design in smaller ceramic packages such as 5.0 x 3.2mm, 3.2 x 2.5mm, etc. The fundamental frequency increases up to 66MHz helps simplify circuit design and is more efficient compared to the old traditional third-overtone circuit complexity.
- Features of E-Beam sealing:
 - ✓ Tight stability and tight tolerance (±10ppm).
 - ✓ Low ESR and high reliability by vacuum package.
 - ✓ Resistance to shock and moisture.
 - ✓ High productivity captured with seam sealing method.
 - ✓ Miniaturization by fine processing of E-Beam.
- LTCC packaging helps reducing size and external components.

ULTRA LOW NOISE SPREAD-SPECTRUM CRYSTAL OSCILLATORS

EMI Protection and Spread-Spectrum Technology:

The FCC and the European Community (under CE Mark EMC Directive) require electronic devices to comply with appropriate radiation emission standards. Other international communities such as Asia and Australia are also following the same rules. Practically every electric device and equipment generate unintended electromagnetic radiation, which will get worse as technology advances, especially with even faster electrical signals required in PC, digital devices and equipment.

With the recent advance in semiconductor and computing technology, (faster clock speeds, lower voltage/power, etc.), coupled with the explosion of the wireless technologies, it is easy to understand why EMC is becoming one of the most important standard requirements in the new-technology world.

In the past, shielding and filtering were the most prevalent method used to control EMI. This method of shielding and filtering can get very expensive. As frequency increases, the effects of transmission line and ground impedance will amplify the radiation, and at the same time wavelength decreases, making shielding and filtering less effective.

The present trend is to control EMI at the source, the single clock oscillator using spread-spectrum technology.

THEORY:

Spread-spectrum is, more or less, frequency modulating the clock signal with a unique waveform. In the frequency domain, this is equivalent to reducing the peak by distributing the energy of each fundamental and harmonic over a wide range. The spread-spectrum method must be controlled and slow compared to the clock rate to guarantee that the change in the clock rate is transparent to the system. Essentially, spread-spectrum is a modulation method where the modulation is measured as a percentage.

For example, a 0.5 percent modulation means that a 100MHz clock is modulated between 99.5MHz and 100.5MHz. This is called a center 0.5 percent modulation, since the 100MHz fundamental frequency remains the center frequency. The designer must keep in mind that both cycle-to-cycle and pea-to-peak jitter must remain within the system's specifications.

Another important factor is the modulation frequency, which is usually in the kilohertz range. This is basically a measure of the rate at which the frequency is swept between 99.5 and 100.5. The linear sweep is predictable and most prevalent.

Overall, the spread spectrum method has allowed system performance to increase without compromising EMI. Using Abracon spread-spectrum clock oscillators will not only reduce packaging, shielding, and design-cycle costs, but also expedite time-to-market of products which otherwise may fail regulatory EMI limits and standards. Abracon ultra low noise series oscillators provide an economical solution to expensive EMI problems.

LOW EMI CRYSTAL CLOCK OSCILLATORS

Spread Spectrum Technology used to reduce EMI has been integrated into industry standard 8 and 14 pin DIP packages and surface mount versions as small as 5 X 7 mm. These products are perfect drop-in replacement clock oscillators where EMI reduction of up to 20 dB is needed.

Typical system designs start out with some fundamental clock source, such as a crystal, ceramic or can oscillator, at some frequency, lets say 48 MHz, which drives a processor, memory, serial/USB interfaces and some front panel controls. The 48 MHz clock is changed into other timing components such as clock multipliers found in PLL based processors, memory controllers, and interface controllers. The original 48 MHz clock quickly becomes 96 MHz or 24 MHz to drive a serial interface. These fundamental and harmonic frequencies can make it very difficult for compliance engineers to achieve certification.

During the design phase, if the proper package and frequency is chosen for the clock source, the flexibility in future modifications is increased. Even after the design phase is done, there will always be hot spots that will require some form of filtering or shielding. If all that is needed is to slow down the rise time of one or two specific nets, but this is not usually the case. If, however, the EMC engineer sees that the agency limits have been exceeded by 10 dB in several higher frequency harmonics, production must wait until compliance is achieved. When this happens, there are 3 possible ways to solve the problem, re-design in an attempt reduce EMI, filter and shield every net that is offending compliance or change the bill of material to call out a Low EMI Clock Oscillator.

SSC takes advantage of the fact that a frequency-modulated carrier will have lower peak energy than a non-modulated carrier. By frequency modulating the carrier, the energy is spread out over a wider range of frequencies, thereby reducing the peak energy contained in any one frequency. Comparing a modulated clock to a non-modulated clock on a spectrum analyzer, it can be seen that the peaks of the modulated clock and harmonic frequencies are lower in relative strength. The difference in relative strength of the energy of the clock is measured in dB. Sweeping the frequency of the fundamental clock back and forth at some rate will cause a reduction in peak energy. The wider the spread the greater the peak energy reduction. To determine how much spread you need for a given application use the simple formula below to calculate the necessary dB reduction. This formula assumes an ideal clock with a 50% duty cycle and only predicts the EMI reduction of odd harmonics.

Calculation for dB reduction:

$$\text{dB} = 6.5 + 9(\text{Log}_{10}(\text{F})) + 9(\text{Log}_{10}(\text{BW}))$$

Where; **F** = Frequency in MHz and **BW** = total % spread (2.5% = .025)

Using a 96 and 480 MHz clock with a 2.5% spread, the theoretical dB reduction would be;

$$\text{dB @ 96 MHz (Fund)} = 6.5 + 17.84 - 14.4 = 9.92$$

$$\text{dB @ 480 MHz (5th)} = 6.5 + 24.13 - 14.4 = 16.21$$

Regulatory agencies control the maximum amount of radiated RF energy. Unwanted RF energy is considered EMI, which causes interference in local receiving equipment such as television, radio, cell phones and pagers.

Agencies, such as the Federal Communications Commission, regulate the amount of radiated energy in terms of voltage, distance and frequency. The FCC has two classes of radiation levels, stated as Class A and Class B. Class A devices are digital devices intended for use in commercial, industrial or businesses and not intended for use by the general public or in the home. Class B digital devices are intended to be used in the home but could also be used elsewhere. In general, Class B levels are more difficult to meet than Class A.

LOW EMI CRYSTAL CLOCK OSCILLATORS

The following chart lists the voltage levels allowed under FCC Rules and Regulations, Part 15, for both Class A at 10 meters and Class B at 3 meters.

Frequency (MHz)	Class "A" (10 meters)		Class "B" (3 meters)	
	uV/m	dB(uV/m)	uV/m	dB(uV/m)
30 - 88	90	39	100	40
88 - 216	150	43.5	150	43.5
216 - 960	210	46.5	200	46
>960	300	49.5	500	54

FCC Class A and B Limits

If the equipment under test exceeds these limits, the excess energy must be reduced to within agency limits. Reducing the excess amount of EMI to just under the agency limits is dangerous because there is no guarantee that the differences in manufacturing and environmental changes might cause the energy to increase slightly. Most companies require a safety margin to ensure that the device always complies with agency limits even when manufacturing processes or environmental conditions change. Reducing a particular offending frequency that is 10 dB, for example, over the limit at the 5th harmonic can be very difficult. The problem is further complicated by a company imposed 4-dB safety margin.

Replacing the original clock source with a Low EMI Clock Oscillator is the most efficient way to systemically reduce EMI by a large amount. Referring to figure 1, the 5th harmonic of a 96 MHz clock has been reduced by greater than 15.5 dB just by replacing the original clock oscillator with a Low EMI Clock Oscillator.

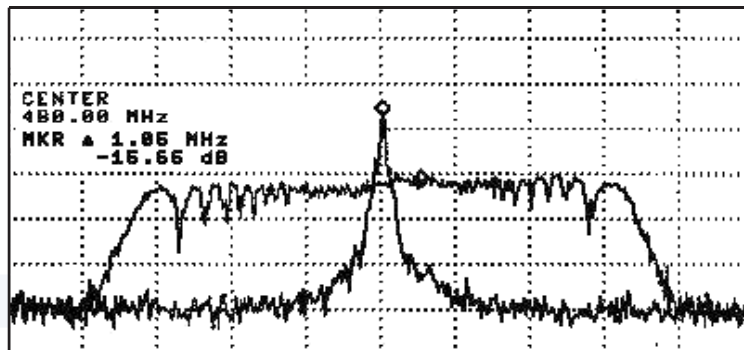


Figure 1.

Low EMI Clock Oscillators ASSM, ACSH, ACSO and ASSL series operate over a frequency range from 4 to 128 MHz at 3.3 and 5.0 volts in commercial and industrial temperature ranges. Products cover a wide range of applications, including automotive, medical, industrial control and computer peripherals such as printer, scanner, copiers and any other digital systems requiring EMI clocking solutions.

For further information on Low EMI Clock Oscillators, including pricing, availability, datasheets, application notes, and peak reduction calculator, contact Abracon Corporation at 1-949-448-7070 or online at www.abracon.com.

LOW EMI CRYSTAL CLOCK OSCILLATORS

MODULATION FREQUENCY

Modulation Frequency is the frequency or rate at which the frequency of the clock sweeps from the peak minimum frequency to the peak maximum and back to the peak minimum frequency again. This parameter frequency is stated in kHz in datasheets and is in the range of 20-150 kHz. There are several conditions that will dictate the maximum and minimum modulation frequency. The minimum modulation frequency should be greater than 20 kHz, which is the above the audio range and lower than 100 kHz. The maximum modulation frequency is determined by several factors including the loop bandwidth of downstream PLL's. The modulation rate of the ACSH and ASSML is in the range of 31.25 kHz to 62.50 kHz. The modulation rate of these devices varies with the operating frequency, but will stay in this range for an operating frequency of 4 MHz to 128 MHz.

The modulation profile of the ACSH / ASSML is pre-programmed and follows a specific pattern, which gives the highest amount of EMI reduction. The modulation profile can be seen on a Time Domain Analyzer, which displays frequency over time. The scans in figure 1, below shows a 6.00 MHz and a 96 MHz profile specific information relating to BW, Modulation Frequency and profile Envelope.

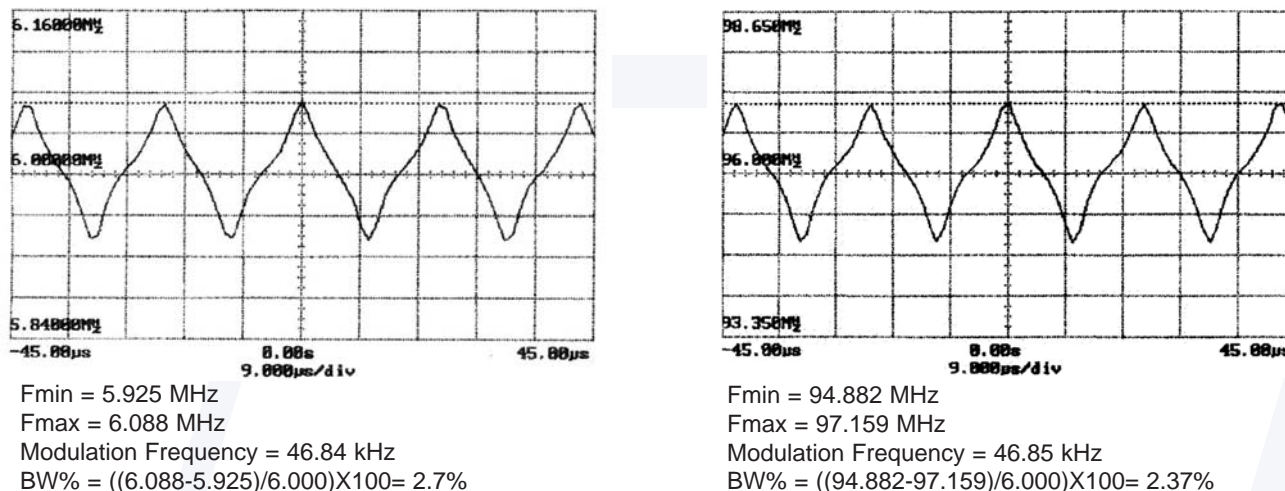


FIGURE 1

BANDWIDTH

Bandwidth is the amount of modulation applied to the original clock frequency. Bandwidth is specified in terms of percentage of the clock frequency. If the frequency of a given clock is 40 MHz and the modulation applied is a total frequency swing of 1.0 MHz, the BW% would be $1/40 = 0.025$ or 2.5%. Generally speaking, the higher the bandwidth the greater the EMI reduction. There are practical boundaries to this statement and the application of large spreads should be used cautiously. A bandwidth of a greater than 5% is extreme and should be tested fully before going to production. The bandwidth of a modulation clock can be measured on a Spectrum Analyzer and more accurately on a Time Domain Analyzer. Applying modulation to the fundamental clock frequency also applies the same amount of BW% spread to the harmonic frequency of that clock. If the fundamental clock frequency is 40.0 MHz, the 3rd harmonic would be 120 MHz and the 5th harmonic would be 200 MHz. In this example, a 2.5% spread at the fundamental frequencies also applies 2.5% spread at the 3rd and 5th harmonics as well. The effect of modulation on EMI reduction at the higher harmonics is greater than at the fundamental frequency; this is because a 2.5% spread at 40 MHz is 1.0 MHz but a 2.5% spread at 120 MHz is 3.00 MHz.

CERAMIC RESONATORS

Why Ceramic Resonators? Ceramic resonators stand between quartz crystals and LC/RC oscillators in regard to accuracy. They offer low cost and high reliability timing devices with improved start-up time to quartz crystals.

Package styles: Abracon offers a wide variety of package styles for ceramic resonators. They come with two or three terminals leaded type or surface-mount type. We also offer the washable industrial grade ceramic resonators with gold flash terminals on the surface-mount types (AWSCR, AWSZT).

Properties: The oscillation of ceramic resonators is dependent upon mechanical resonance associated with their piezoelectric crystal structure. These materials (usually Barium Titanate or Lead-Zirconium Titanate) have large dipole movement, which causes the distortion or growth of the wafer by an applied electric field.

Oscillation mode: The ceramic resonator oscillates in thickness-shear vibration mode for Fundamental frequencies (typical less or equal than 8MHz) and thickness-longitudinal vibration mode for third-overtone mode (above 8MHz to 50MHz).

Frequency range: The available frequency range varies from 182kHz to 50MHz.

Frequency tolerance at 25°C: The maximum allowable frequency deviation from the nominal frequency at room temperature. Frequency tolerance is expressed in percent. Typical frequency tolerance is $\pm 0.5\%$ max. Frequency tolerance can be controlled tighter on built-in capacitance type.

Frequency stability: The maximum allowable deviation compared to the measured frequency at 25°C over the temperature window, i.e. -20°C to $+80^{\circ}\text{C}$ or -40°C to $+125^{\circ}\text{C}$. Standard frequency stability is $\pm 0.3\%$.

Resonant Impedance: The net impedance of the ceramic resonator at resonant frequency. Ceramic resonators have superior resonant impedance than quartz crystal, which offer much better start-up time.

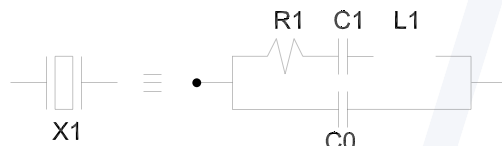
Aging: The relative frequency change over 10 years period. The aging is $\pm 0.3\%$ max. over 10 years.

Load capacitance CL: Since ceramic resonators have very large parallel resonance area and frequency is very sensitive to load capacitance, exact value of load capacitance must be specified. This process is usually been done through IC matching and characterization. Please contact Abracon for details.

Equivalent circuit: The equivalent circuit of the ceramic resonator is similar to the quartz crystal, but motional parameters are very different.

See figure 1 below:

For 4MHz: $L1 = 385\mu\text{H}$, $C1 = 4.4\text{pF}$, $C0 = 36.3\text{pF}$, $R1 = 8\Omega$, $Q = 1134$, $\Delta F = 228\text{kHz}$.



Manufacturing Process: Material Mixing – Calcination – Milling – Spray Dry Seving – Pressing – Sintering – Printing – Sintering – Poling – Slicing – Sputtering – Dicing – Wire forming – Soldering – Lead frame insert – Wax coating – Epoxy coating – Epoxy curing – Inspection – Packaging – Shipping.

Why do ceramic resonators have lower cost than quartz crystals?: Because ceramic resonators have high mass production rate, small size, no need for adjustment.

Properties of automotive and industrial grade ceramic resonators: Abracon offers a new line up of automotive and industrial grade ceramic resonators operating at -40°C to $+125^{\circ}\text{C}$, in supplement to its current consumer grade products which are operating at -20°C to $+80^{\circ}\text{C}$. The automotive grade, which offers excellent frequency tolerance, stability, provides a reliable start-up over the wide temperature. The parts can be ultrasonic (1 minute at 60°C , frequency 28kHz, output 20W/L) or rinse washed with water for a limited time and must be dried completely to guarantee performance.

IC characterization for ceramic resonators: Due to ceramic resonators' properties, IC matching must be studied and performed to satisfy oscillation conditions. The following possible causes may occur if IC matching was not performed:

- In-circuit oscillation frequency off tolerance limit.
- Not-start-up or start-up at an unwanted frequency.
- Stop oscillating or oscillating off limits over temperature.
- Oscillation at overtone mode.
- Poor aging due to over power driving.

Also, there is possibility between frequency correlation between test jig and customer IC. The circuits below show an example between IC characterization of a TMP87P808M and correlation of in-house test jig using CD4069UBE.

CERAMIC RESONATORS

IC characterization steps:

Frequency correlation between customer's IC and standard IC tested.

Temperature characteristics of oscillating frequency.

Temperature characteristics of oscillating voltage.

Rise time vs. Vdd characteristics.

Oscillating frequency vs. Vdd characteristics.

Oscillating voltage vs. Vdd characteristics.

Oscillating frequency vs. C1 values (C2 constant)

Oscillating frequency vs. C2 values (C1 constant)

Oscillating voltage vs. C1 values (C2 constant)

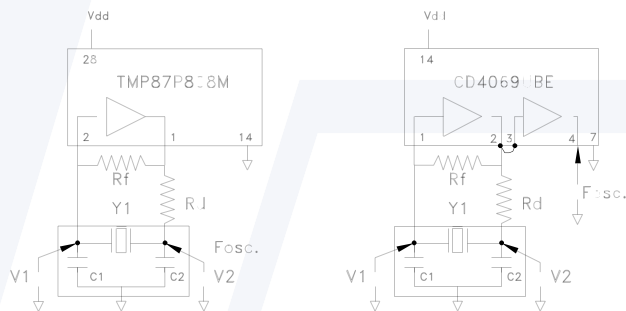
Oscillating voltage vs. C2 values (C1 constant)

Oscillating frequency vs. CL value (C1 = C2)

Oscillating voltage vs. CL value (C1 = C2)

Rise time vs. CL characteristics (C1 = C2)

Starting voltage vs. CL characteristics (C1 = C2)



Polarization on ceramic resonators: Both quartz crystals and ceramic resonators do not have polarity since leads can be mounted interchangeably. However, since ceramic resonator has much wider trim sensitivity vs. load capacitors value $\pm 20\%$, we recommend mounting in the same way as we do the characterization.

IC characterization request: Abracon will offer our customer, in most cases, IC characterization at no cost. It is very important to have this process done in early stage of design and board evaluation. However, please allow us extra time to complete and submit the report. We need the following information to send along when submitting a request:

Application. Please be specific either automotive or consumer grade applications.

Package style (leaded or surface-mount).

Electrical parameters.

Estimate annual usage.

Pilot run and production date.

IC part number and manufacturer

Applied voltage and tolerance, e.g. 12Vdc $\pm 10\%$

Operating temperature.

2 to 5 bulk IC samples or the actual PCB with components

mounted in oscillator section. The PCB is preferred so that parasitic effects on the board can be taken into account.

A top view pin assignment for the package of the IC samples.

Attached schematic shown values of components values such as Rd, Rf, C1, C2, etc.

Specify date needed.

Name and E-mail contact.

As soon as we received the complete information and materials as specified, we will submit the report and recommendations within 4 to 6 weeks.

LAYOUT HINTS:

When you design circuit on a PCB, please take the following considerations:

Please design the trace length as short as possible.

Try to avoid thin line on resonator traces ($< 0.010''$). Design as wide as possible.

If noise occurs, please insert EMI filter with serial mode between XOUT pin and resonator or between capacitor and GND.

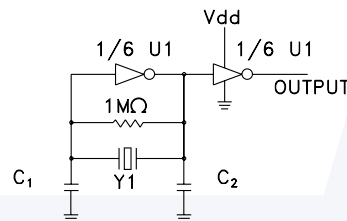
TEST CIRCUITS:

We used standard CMOS and HCMOS ICs in our test set-up.

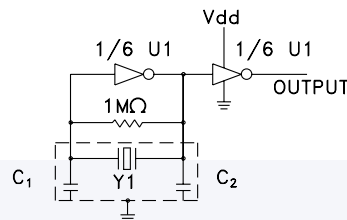
CMOS: CD4069UBP tested at 12VDC for $F < 8\text{MHz}$

HCMOS: TC74HCU04 tested at 5VDC.

We used standard $30\text{pF} \pm 20\%$ capacitors for C1 and C2, unless otherwise specified.



- U1: CD4069UB
74HCU04 ($> 8\text{MHz}$)
- Y1: RESONATOR
- C1 C2 : $30\text{pF} \pm 20\%$



- U1: CD4069UB
74HCU04
- Y1: RESONATOR
- C1 C2 : $30\text{pF} \pm 20\%$ (Built-in)

QUARTZ CRYSTAL OSCILLATORS GLOSSARY OF TERMS

Nominal frequency: The center or nominal output frequency of a crystal oscillator.

Package: Crystal oscillators are packaged in various styles from lead through holes to surface-mount types. Various sizes and functions are suitable for different applications.

Frequency tolerance: The deviation from the nominal frequency in terms of parts per millions (ppm) at room temperature. ($25^{\circ} \pm 5^{\circ}\text{C}$)

Frequency range: The frequency band that the oscillator type or model can be offered.

Frequency stability: The maximum allowable frequency deviation compared to the measured frequency at 25°C over the temperature window, i.e., 0°C to $+70^{\circ}\text{C}$. Typical stability is $\pm 0.01\%$ (± 100 ppm).

Operating temperature: Temperature range within which output frequency and other electrical, environmental characteristics meet the specifications.

Aging: The relative frequency change over a certain period of time. This rate of change of frequency is normally exponential in character. Typically, aging is ± 5 ppm over 1 year maximum.

Storage Temperature: The temperature range where the unit is safely stored without damaging or changing the performance of the unit.

Frequency vs. Power Supply Variation: Maximum frequency change allowed when the power supply voltage is changed within its specified limits (typical $\pm 10\%$ in VCC or $\pm 5\%$ change).

Supply Voltage (Vdd max): The maximum voltage which can safely be applied to the Vcc terminal with respect to ground. Maximum supply voltage for TTL is 5.5V and for HCMOS is 7V.

Input Voltage (VIN): The maximum voltage that can be safely applied to any input terminal of the oscillator.

Output HIGH voltage (VOH): The minimum voltage at an output of the oscillator under proper loading.

Output LOW voltage (VOL): The maximum voltage at an output of the oscillator under proper loading.

Input HIGH voltage (VIH): The minimum voltage to guarantee threshold trigger at the input of the oscillator.

Input LOW voltage (VIL): The maximum voltage to guarantee the threshold trigger at the input of the oscillator.

Supply Current (Icc): The current flowing into Vcc terminal with respect to ground. Typical supply current is measured without load.

Symmetry or Duty Cycle: The symmetry of the output waveform at the specified level (at 1.4V for TTL, at $1/2$ Vcc for HCMOS, or $1/2$ waveform peak level for ECL). See Fig. 1

$$\text{SYM} = \frac{t_H}{T} \times 100 (\%)$$

Fan Out: The measure of driving ability of an oscillator, expressed as the number of inputs that can be driven by a single output. It can be represented by an equivalent load capacitance (CL) or a TTL load circuit consisting of diodes, load resistor, and a capacitor.

Rise Time (Tr): Waveform rise time from Low to High transition, measured at the specified level

- 10% to 90% for HCMOS,
- 20% to 80% for ECL
- 0.4V to 2.4V for TTL.

Fall Time (Tf): The waveform fall time from High to Low transition, measured at the specified level

- 90% to 10% for HCMOS,
- 80% to % for ECL
- 2.4V to 0.4V for TTL.

Jitter: The modulation in phase or frequency of oscillator output.

HCMOS/TTL Compatible: The oscillator is designed with ACMOS logic with driving capability of TTL and HCMOS loads while maintaining minimum logic HIGH of the HCMOS.

Tristate Enable: When the input is left OPEN or tied to logic "1", the normal oscillation occurs. When the input is Grounded (tied to logic "0"), the output is in high impedance state. The input has an internal pull-up resistor thus allowing the input to be left open.

Output Logic: The output of an oscillator is designed to meet various specified logic states, such as TTL, HCMOS, ECL, Sine, Clipped-Sine (DC cut).

Harmonic Distortion: The non-linear distortion due to unwanted harmonic spectrum component related with target signal frequency. Each harmonic component is the ratio of electric power against desired signal output electric power and is expressed in terms of dBc, i.e. -20dBc. Harmonic distortion specification is important especially in sine output when a clean and less distorted signal is required.

Phase Noise: The measure of the short-term frequency fluctuations of the oscillator. It is usually specified as the single side band (SSB) power density in a 1Hz bandwidth at a specified offset frequency from the carrier. It is measured in dBc/Hz.

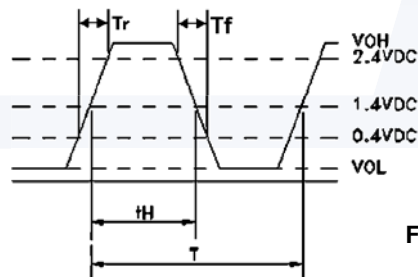


Figure 1.

$$\text{Symmetry} = \frac{t_H}{T} \times 100\%$$

Stand By: A function that temporarily turns off the oscillator and other dividers to save power. Logic "0" will enable stand by mode. The disable current at stand by mode varies from a few micro-amperes to tens of micro-amperes (5μA typical). Because oscillation is halted, there is a maximum of 10 ms (same amount of start-up time) before output stabilizes.

QUARTZ CRYSTAL OSCILLATORS

Q: Introduction to Abracon Programmable Oscillators:

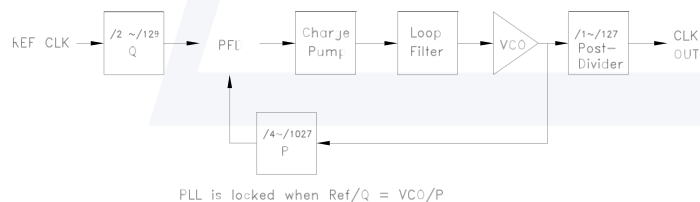
A: Abracon offers quick-turn programmable oscillators in four different package styles; the ceramic package 7.0 x 5.0 x 1.6 mm, plastic molded package similar to Epson SG-8002, and the 14 pin and 8 pin dip packages. The single PLL architecture with EPROM programmable generates a custom frequency derived from an internal crystal between 10MHz to 25MHz. The main advantages of the programmable oscillators are:

- Easy customization and fast turnaround.
- Wide frequency ranges 1MHz to 133MHz.
- Programming accuracy > 6 digits.
- Output control Synchronous or Asynchronous.
- Output levels CMOS or TTL.
- Fast rise and fall times.
- Fast programming time < 5 seconds per unit.
- Low skew, low jitter, high accuracy outputs.
- Enables design flexibility and easy of use.
- Powerdown and output enable options available.
- Configurable 5V or 3.3VDC operation in seconds.
- Reprogrammable for quick design changes (applied to blank only).
- Extended temperature -40°C to +85°C with good frequency vs. temperature characteristics.

Q: What is PLL technology?

A: A PLL allows a frequency to be generated from any other frequency, where:

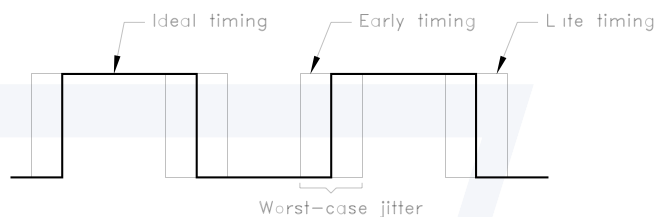
$$CLK\ OUT = \frac{REF.\ CLK * P/Q}{Post-Divider}$$



Q: What is jitter?

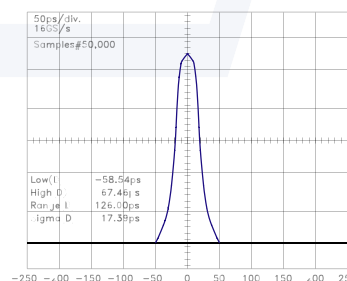
A: Jitter is the uncertainty or short-term variations of a digital waveform timing from their ideal positions in time.

The waveform transition could be too early or too late compared to the ideal waveform timing.



Q: How to measure jitter?

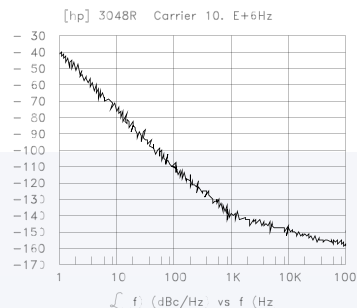
A: We use LeCroy digitizing oscilloscope with jitter timing software for jitter measurement and analysis. The scope must have the bandwidth at least five times the frequency of the waveform since the waveform jitter is measured as each rising cycle crosses the threshold voltage. The larger number of continuous cycles the more accurate is the jitter distribution. Jitter is measured in cycle-to-cycle



(or absolute jitter) or one sigma jitter (rms.) using the histogram analysis. Unit of jitter is ps.

Q: Can phase noise be improved in designs?

A: Yes. Crystal oscillators can be designed to minimize their phase noise characteristics. Special applications such as wireless require best phase noise both at far-end and close-end. Crystal parameters and mounting methods directly affect close-end phase noise 300Hz offset from carrier. The oscillator front-end and output buffer



QUARTZ CRYSTAL OSCILLATORS

Q: Why the Overall frequency stability is specified in crystal oscillators but not in crystals?

A: The crystal oscillator is typically used as a master clock for the microprocessor and its parameters are not affected by the internal characteristics of the microprocessor such as variation in load capacitance and other variables that could affect the change in frequency at room and over temperature. The overall frequency stability in crystal oscillators is typically $\pm 100\text{ppm}$ max. and includes frequency calibration at 25°C , over temperature, frequency changes due to load, supply, aging, vibration, and shock.

Q: What is the start-up time?

A: Start-up time is the delay time between the oscillation starts from noise until it reaches its full output amplitude when power is applied. The supply voltage must be applied with a defined rate or rise. The start-up time varies from microseconds to milliseconds depending on frequency, ASIC speed and logic. Please see figure 1.

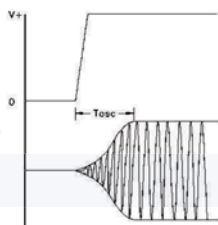


Figure 1

Q: What is Tristate Enable/Disable mode?

A: When the voltage at the control pin is set to a logic low "0", the output is in Tri-state mode that is High Impedance. The disabled current is usually lower than its normal operating current but not completely cut-off as it was seen in the Stand-by mode, where the oscillation is shut down completely. There is an internal pull-up resistor between control pin and supply (typically $100\text{k}\Omega$), therefore the control pin can be left open (floating) if unused.

Q: What is jitter and how to specify its maximum value?

A: Jitter is noise caused by many sources in crystal oscillators. Major sources of noise are:

- Power supply noise.
- Integer multiples of the signal source frequency (harmonics).
- Load and termination conditions.
- Amplifier noise.
- Circuit configuration (PLLs, Multiplier, Overtone, etc.)

The following methods can be used to suppress the noise conditions in the above sources:

- Make sure that the power supply noise is filtered by using by pass capacitors, chip beads, or RC filters.
- If jitter is critical in some applications, especially for high-frequency noise, use low harmonics outputs or sine output.
- Make sure that load and termination conditions are optimized to avoid reflected power back to its output.
- Typically, PLLs, Multiplier or Programmable designs produce higher jitter than the conventional fundamental design.

It is very important to understand the jitter requirements from the application to specify the right specification for crystal oscillators.

We can classify two types of jitters:

- Cycle to cycle jitter
- Period jitter.

CYCLE TO CYCLE JITTER

The Cycle to cycle jitter is the maximum difference in time between several measured periods. Usually a minimum of ten (10) cycles is used where T1 to T10 were recorded. See fig. 2.

Jitter = Maximum Delta (Ts)

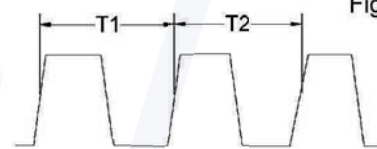


Figure 2

PERIOD JITTER.

The period jitter is the maximum change of a clock edge. It is usually expressed as peak-to-peak jitter and can be converted to rms value by multiplying to $(0.5) \times (0.707)$. The period jitter can only be measured at each cycle but not multiple cycles. See figure 3.

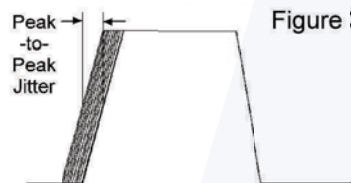
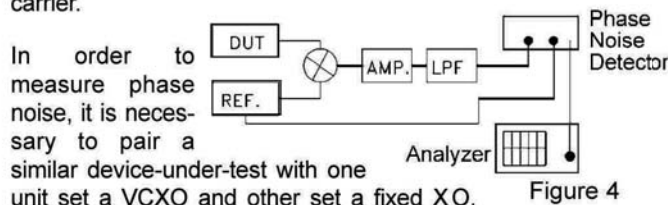


Figure 3

Typical jitter recorded in Abracon oscillators varies from 20ps to 60ps rms.

Q: What is phase noise and how to measure it?

A: Phase noise is the expression of noise in the frequency domain. It is a measure of the short-term frequency fluctuations of the oscillator. It is usually specified as the single sideband power density in a 1Hz bandwidth at a specified offset frequency from the carrier.



In order to measure phase noise, it is necessary to pair a similar device-under-test with one unit set a VCXO and other set a fixed XO.

Please see block diagram in figure 4. Typical phase noise in Abracon VCXO and oscillators:

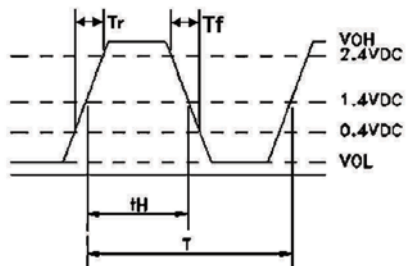
OFFSET FREQUENCY (Hz)	PHASE NOISE (dBc/Hz)
10	-70
100	-110
1,000	-125
10,000	-150
100,000	-160

QUARTZ CRYSTAL OSCILLATORS

CMOS RISE AND FALL TIMES

The rise and fall time on the CMOS technology depends on its speed (CMOS, HCMOS, ACMOS, BICMOS), the supply voltage, the load capacitance, and the load configuration. Typical rise and fall time for CMOS 4000 series is 30ns, HCMOS is 6ns, and for ACMOS (HCMOS, TTL compatible) is 3 ns max.

Typical rise and fall time is measured between 10% to 90% of its waveform level.



OUTPUT WAVEFORM
Figure 1

ACMOS OUTPUT TERMINATION TECHNIQUES

Due to the fast transition time of the ACMOS (HCMOS/TTL compatible) device, proper termination techniques must be used when testing or measuring electrical performance characteristics.

Termination is usually used to solve the problem of voltage reflection, which essential cause steps in clock waveforms as well as overshoot and undershoot. Such effect could result in false clocking of data, as well as higher EMI and system noise.

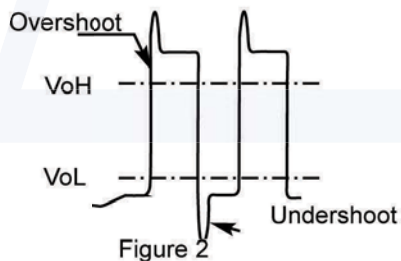


Figure 2

Termination is required also because of the length of the trace on the PC board and its load configuration.

There are three general methods of terminating a clock trace, which is a process of matching the output impedance of the device with the line impedance:

- 1) Series termination;
- 2) Pull-up/Pull-down termination;
- 3) Parallel-AC termination

METHOD 1:

Series termination (Fig. 3)

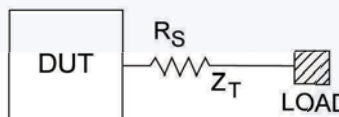


Figure 3
 $R_s \geq Z_T - R_o$

In series termination, a damping resistor is placed close to the source of the clock signal. Value of R_s must satisfy the following requirement:

METHOD 2:

Pull-Up / Pull-Down Resistors (Fig. 4)

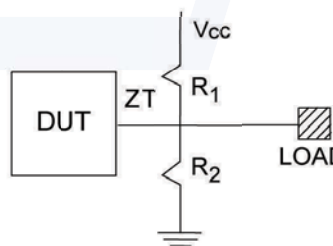


Figure 4

In pull-up/pull-down termination, the Thevenin's equivalent of the combination is equal to the characteristics impedance of the trace. This is probably the cleanest, and results in no reflections, as well as EMI.

$$R_T \sim Z_T$$

METHOD 3:

Parallel AC Termination (Fig. 5)

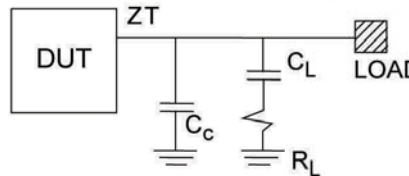


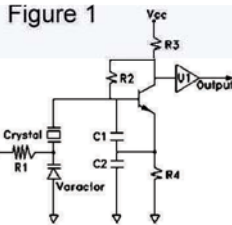
Figure 5

In parallel AC termination, a R-C combination is placed at the load. The value of the capacitor must be chosen carefully, usually smaller than the 50pF. This termination is not recommended because it will degrade the rise and fall time of the clock, although it draws no DC current.

VCXOs and TCXOs

Q: What are the factors that affect frequency pullability?

A: The frequency pullability or deviation in VCXO is the change in the output frequency with respect to change in control voltage. Pullability is usually specified as minimum; however, in some applications, a maximum pulling value is also specified to avoid circuit instability. Please refer to figure 1 for a typical Colpitts VCXO circuit:



Some major factors that affect the frequency deviation in VCXO:

- Load capacitance value C1 and C2.
- Frequency.
- Crystal characteristics (C1, C0/C1, size)
- Varactor type and capacitance.
- Voltage control Vc.
- Operating temperature.

The frequency pullability can be increased either by using a low capacitance with sharp slope varactor, connect in series another varactor or an inductor, adjusting load capacitor values C1 and C2, or increasing control voltage.

Be very careful when considering any above methods because it may create circuit instability which has a severe effect on jitter, linearity, unwanted modes, frequency hysteresis, or frequency shift over temperature.

Q: What is the typical input impedance?

The input impedance is a function of modulation frequency. Its minimum input impedance is 50kW at 10kHz.

Q: What is the transfer function?

A: The transfer function is the direction of change in frequency versus the change in control voltage. Most applications require a positive transfer function, which the frequency rises when increasing control voltage.

Q: What is linearity and what are the factors that affect it?

A: Linearity is the deviation from the best straight-line slope of the frequency versus control voltage curve. The typical linearity in Abracon VCXO is ±10% maximum for standard pullability. Larger pulling may worsen the linearity.

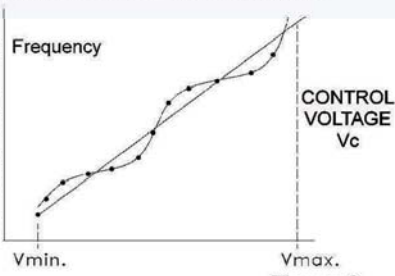


Figure 2

Q: What is the modulation bandwidth?

A: The modulation bandwidth is the minimum ±3dB bandwidth frequency, relative to a 1kHz to 10kHz modulation frequency. Unless otherwise specified as default, other values of modulation bandwidth and frequency must be specified when ordering.

Q: What is the control voltage?

A: The control voltage is the external voltage applied to the input of the VCXO. It consists of a minimum, a maximum, and a center voltage. The center control voltage is the nominal voltage that sets the oscillation frequency to its minimal value.

Standard control voltages:

Vc min = 0.5Vdc; Vc max. = 4.5Vdc; Vc center = 2.5Vdc ± 0.5V

Q: What is a TCXO?

A: A TCXO (Temperature-Compensated Crystal Oscillator) is a crystal oscillator that has a high-precision crystal, a temperature-compensated network. There are several methods to design a compensated network, which could vary from simple, less expensive to, complicate and very expensive:

- **Method 1:** Thermistor/Capacitor networks (Direct compensation). Lowest cost, no varactor needed.
- **Method 2:** Traditional thermistor network.
- **Method 3:** Analog Polynomial Generator
- **Method 4:** Digitally segmented analog
- **Method 5:** Digital compensation
- **Method 6:** Digital compensation with DAC voltage summers.

Figure 3 shows a traditional thermistor network:

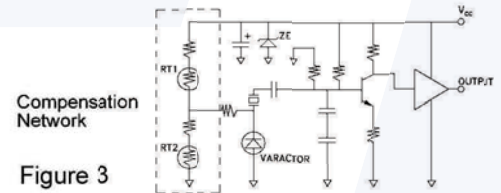


Figure 3

Q: Why and when we need to use a TCXO?

A: We need to use a TCXO when the frequency stability of the oscillator falls beyond the design limitation of a standard simple (fixed) crystal oscillator which is typically less than ±5ppm over a standard or extended temperature window. The TCXO costs more due to its complex circuit and manufacturing.

Q: Why there is an internal trimmer or control voltage on a TCXO?

A: The purpose of the internal trimmer (variable capacitor) or a control voltage is to re-adjust the frequency to its nominal frequency for aging compensation or initial setting. The internal trimmer is accessible via a hole on top of the TCXO can and can be adjusted with a special tool. The control voltage can be set with a voltage divider or an external voltage. Both methods of adjustment usually can not produce large frequency deviation rather than 5 to 15ppm enough to offset the frequency due to standard aging.

Q: How to specify frequency stability on a TCXO?

A: Unless otherwise specified, the frequency stability on a TCXO is specified as follows:

- Due to temperature change: ± 2.5ppm @ -20°C to +70°C
- Due to aging: ± 1ppm per year max.
- Due to supply voltage (±5%): ± 0.3ppm max.

The frequency drift due to temperature change is referred to nominal frequency set at 25°C.

MONOLITHIC QUARTZ CRYSTAL FILTERS

Holder: A case housing a thin piece of quartz crystal with vacuum-evaporated metal electrodes and terminals for connections.

Nominal Frequency: Normally this refers to the nominal value of the center frequency given in the specifications, to which other frequencies may be referred. Nominal frequency usually indicates the Center Frequency (F_0) and Carrier Frequency (F_c).

Pass Bandwidth: The pass bandwidth in which the attenuation is equal to or less than a specified value insertion loss.

Stop Bandwidth: The stop bandwidth in which the attenuations are equal to or greater than specified values in the stop band attenuation.

Ripple: The ripple (in pass band) is the difference between the maximum and minimum attenuation within a passband.

Insertion Loss: The logarithmic ratio of the power delivered to the load impedance before insertion of the filter to the power delivered to the load impedance after insertion of the filter.

Attenuation Bandwidth: The frequency width at the value that assures the relative attenuation is of the same value or higher than the specified attenuation.

Attenuation Guaranteed: The maximum attenuation guaranteed at the specified frequency range.

Termination Impedance: Either of the impedance presented to the filter by the source or by the load, and described the resistive portion (R_t) and the parallel capacitive portion (C_t) including stray capacitance.

Spurious Response: Minimum attenuation caused by extraordinary response in the stopband. Spurious response usually appears at a frequency higher than the center frequency.

Group Delay distortion: The difference between the maximum and minimum group delay within pass bandwidth unless otherwise specified.

Balanced Type and Unbalanced Type: A balanced type is one in which a pair of terminals is not connected to the case. An unbalanced type is one in which one of a pair of terminals is connected to the case.

CRYSTAL FILTERS TEST SET-UP

The termination impedance presented by the source or by the load is either represented by a resistor and a capacitor (capacitive type) or by a resistor and a "negative" capacitor (inductive type). For a capacitive type, specified value of capacitor as given in table can be used in the test circuit. For an inductive type ("negative capacitance"), a L-C network is required to compensate the negative capacitance.

TESTING CONFIGURATION

Two pole filters are cascaded to produce four, six, eight or more pole filter responses with the addition of coupling capacities between two pole sections.

Figure 2
4 Pole MCF

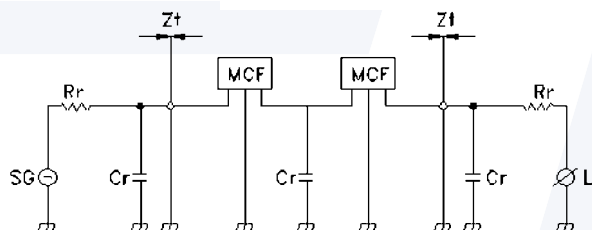
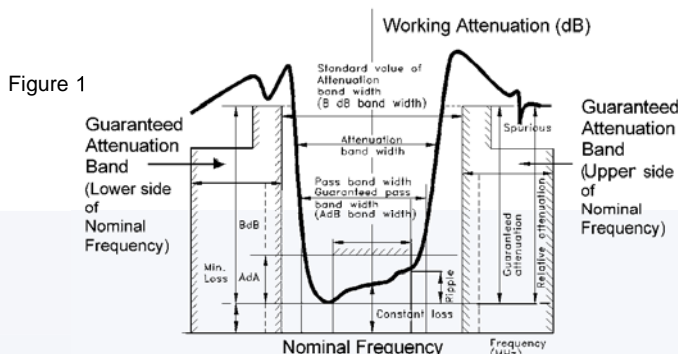
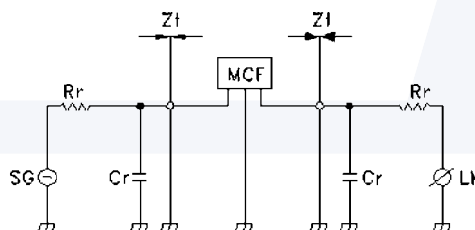


Figure 3
4 Pole MCF



NOTES: (1) AdB: Attenuation which specifies the band width.
(2) BdB: Attenuation which specifies the Attenuation Band Width.

APPLICATIONS

Crystal filters have high stability temperature characteristics and have narrow band, low loss and good attenuation bandwidth. They are widely used in mobile communications systems, mobile and cordless telephones, pagers and radios. Abracon will manufacture crystal filters per custom specifications, including termination impedance, pass band width and attenuation band width.