

i.MXS Development Kit

User's Guide

1 Introduction

The i.MXS Development Kit is designed to operate software applications using the MC9328MXS (i.MXS) applications processor. This User's Guide provides the connection and operation of the i.MXS Reference Board to the i.MXS.

Major features of the i.MXS Reference Board include:

- 100 MHz Freescale MC9328MXS CPU with 16K I-Cache and 16K D-Cache
- 32Mbyte 16-bit Wide SDRAM
- 8 MByte 16-bit Wide NOR Flash
- USB Device Interface
- RS-232 for Debug Serial Port
- Standard 20-Pin JTAG Header
- 2.5" 320 × 240 TFT LCD Panel
- Whole system can be powered by USB

The i.MXS Reference Board includes 5 interface ports that support application software, debugging, or optional memory. An LCD display is provided.

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Figure 1 illustrates the functional blocks of the i.MXS Reference Board.

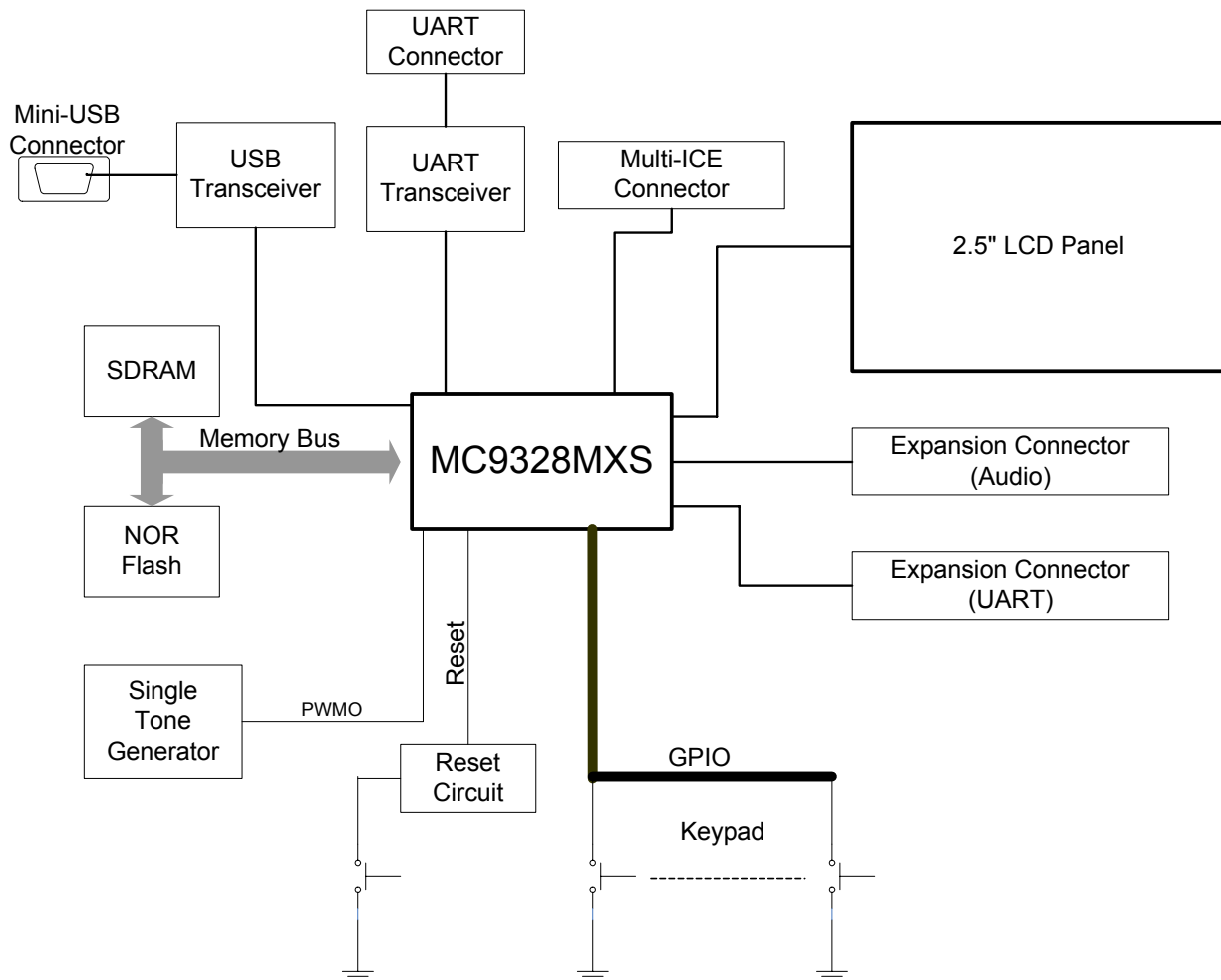


Figure 1. Functional Block Diagram of the i.MXS Reference Board

2 Memory

Table 1 provides the Memory Map of the i.MXS Reference Board. Each of the memory devices are discussed in the following sub-sections.

Table 1. i.MXS Reference Board Memory Map

Memory Device	Chip Select	Address Range (Hex)	Actual Memory Size
NOR Flash	CS0	0x1000 0000 – 0x107F FFFF	8 MByte
SDRAM	CS2 (CSD0)	0x0800 0000 – 0x09FFF FFFF	32 Mbyte

2.1 8 Mbyte NOR Flash

The i.MXS Reference Board uses an Intel StrataFlash[®] 28F640 device for boot memory and it is connected to CS0 of i.MXS.

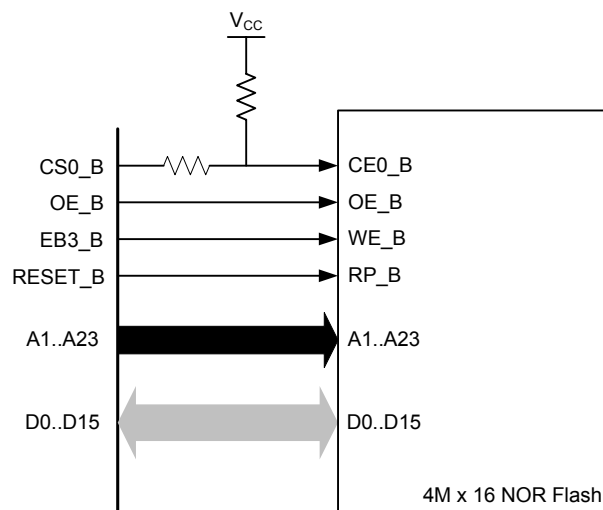


Figure 2. 8 Mbyte NOR Flash

2.2 32 Mbyte SDRAM

The i.MXS Reference Board uses one 16M × 16 PC100 of faster SDRAM for system memory.

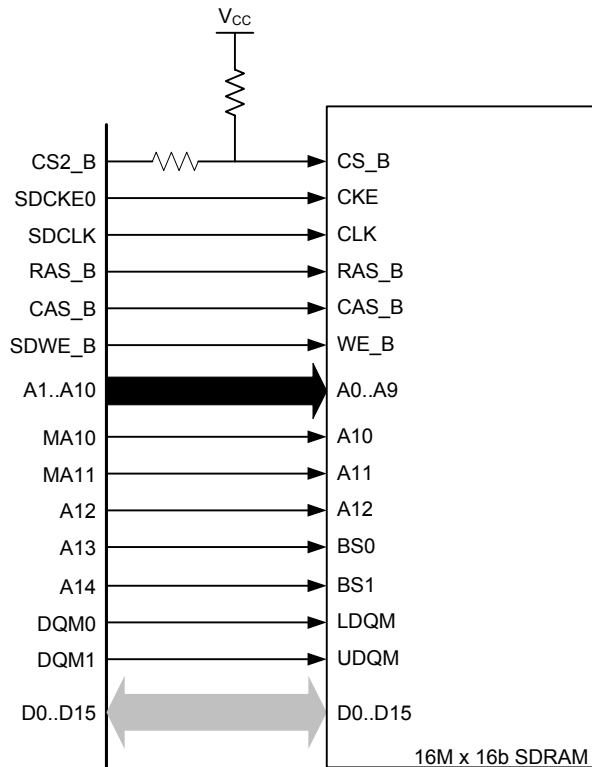


Figure 3. 32 Mbyte SDRAM

3 Power

The i.MXS Reference Board accepts a nominal input voltage of 5V, from either the power jack or the USB port. Make the selection using the power slide switch next to the power jack. When the slide switch set to the right, the board will be powered by the USB port. When set to left, the board will be powered through the power jack.

4 Boot Mode

The 2-way DIP switches (S11) on the board allow you to choose between NOR Flash boot mode and bootstrap mode of i.MXS. [Table 2](#) provides the bootstrap mode selection options.

Table 2. i.MXS Bootstrap Mode Selection

Switch 1	Switch 2	i.MXS Boot Mode
On	On	i.MXS bootstrap mode
On	Off	Reserved
Off	On	Reserved
Off	Off	Boot from 16-bit NOR Flash

5 Interfaces

5.1 UART Daughter Card Expansion Connector (Optional)

UART and SSI signals from i.MXS are available at Connector P5 on the i.MXS Development Kit. This connector enables developers to connect the kit to an external UART daughter card.

Table 3. Bluetooth Connections to P5

Pin	Signal Name	Pin	Signal Name
1	UART2_RXD	11	GND
2	UART2_TXD	12	NC
3	UART2_CTS	13	NC
4	UART2_RTS	14	NC
5	GND	15	NC

5.2 Digital Audio Signals Connection (Optional)

SSI and I²C signals from i.MXS are available at connector P6 to add external audio capability to the board. [Table 4](#) provides the digital audio signal connections to P6.

Table 4. Digital Audio Signal Connections to P6

Pin	Signal Name	Pin	Signal Name
1	SSI_RXCLK	11	SSI_RXDAT
2	GND	12	VCC
3	SSI_TXCLK	13	PB19
4	GND	14	NC
5	SSI_TXDAT	15	PB18
6	NC	16	+5V
7	SSI_TXFS	17	I2C_SDA
8	VCC	18	+5V
9	SSI_RXFS	19	I2C_SCL
10	VCC	20	+5V

5.3 Keypad Interface

There are a total of 10 general purpose keys available on the i.MXS Development Kit. The 10 keys are connected directly to 10 separate GPIO pins of i.MXS as show in [Table 5](#).

Table 5. Keypad Interface to GPIO

Key	i.MXS Signal
S1	PB12
S2	PB11
S3	PB10
S4	PB9
S5	PB8
S6	PB17
S7	PB16
S8	PB15
S9	PB14
S10	PB13

5.4 QVGA TFT Display

The i.MXS Development Kit is equipped with an AUO A025DL02 QVGA 2.5" TFT panel. Please refer to the schematics for the detailed connection of the panel to i.MXS. Please note that the panel is being configured as 16-bit (RGB 5-6-5) on the i.MXS Development Kit.

5.5 USB Connector

The USB connector is P1. [Figure 4](#) illustrates the pin assignments and [Table 6](#) provides the signal descriptions for this connector.

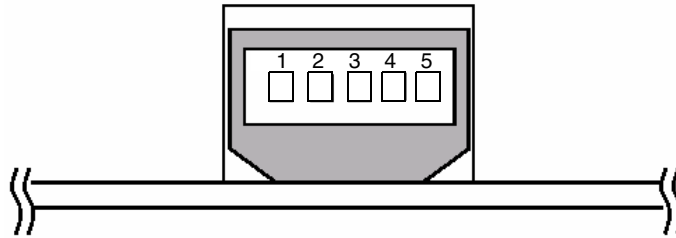


Figure 4. USB Connector P1

Table 6. USB Connector P1 Pin Assignments

Pin	Mnemonic	Signal
1	VBUS	VBUS
2	D-	USB data minus
3	D+	USB data plus
4	NC	No connection
5	GND	Ground

5.6 UART Connector

Connectors P3 is the i.MXS UART connector. [Figure 5](#) illustrates the pin assignments and [Table 5](#) provides the signal descriptions.

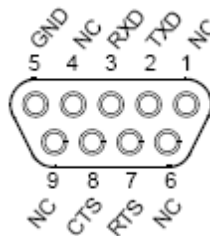


Figure 5. UART Connector P3

Table 7. UART Connector P3 Signal Descriptions

Pin	Mnemonic	Signal
1, 4, 6, 9	NC	No connection
2	TXD	Transmitted data—RS232 serial data output signal
3	RXD	Receive data—serial data input signal
5	GND	Ground

Table 7. UART Connector P3 Signal Descriptions (continued)

Pin	Mnemonic	Signal
7	RTS	Ready to send—active positive, RS232 input signal
8	CTS	Clear to send—active positive RS232 output signal

5.7 Multi-ICE[®] Connector

Connectors P4 is the i.MXS Multi-ICE connector. Figure 6 illustrates the pin locations and Table 6 provides the signal descriptions.

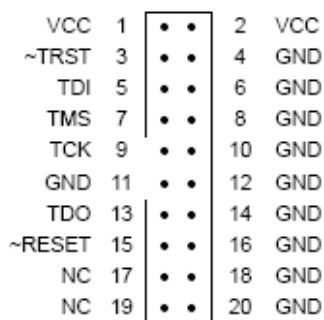


Figure 6. Multi-ICE P4 Connector

Table 8. Multi-ICE Connector P4 Signal Description

Pin	Mnemonic	Signal
1,2	VCC	3 V Power
3	~TRST	Target Reset—Active-low output signal that resets the target.
4, 6, 8, 10 – 12, 14, 16, 18, 20	GND	Ground
5	TDI	TEST DATA INPUT—Serial data output line, sampled on the rising edge of the TCK signal.
7	TMS	TEST MODE SELECT—Output signal that sequences the target's JTAG state machine, sampled on the rising edge of the TCK signal.
9	TCK	TEST CLOCK—Output timing signal, for synchronizing test logic and control register access.
13	TDO	JTAG TEST DATA OUTPUT—Serial data input from the target.
15	~RESET	RESET—Active-low reset signal.
17, 19	NC	No connection

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